ISLPED '09

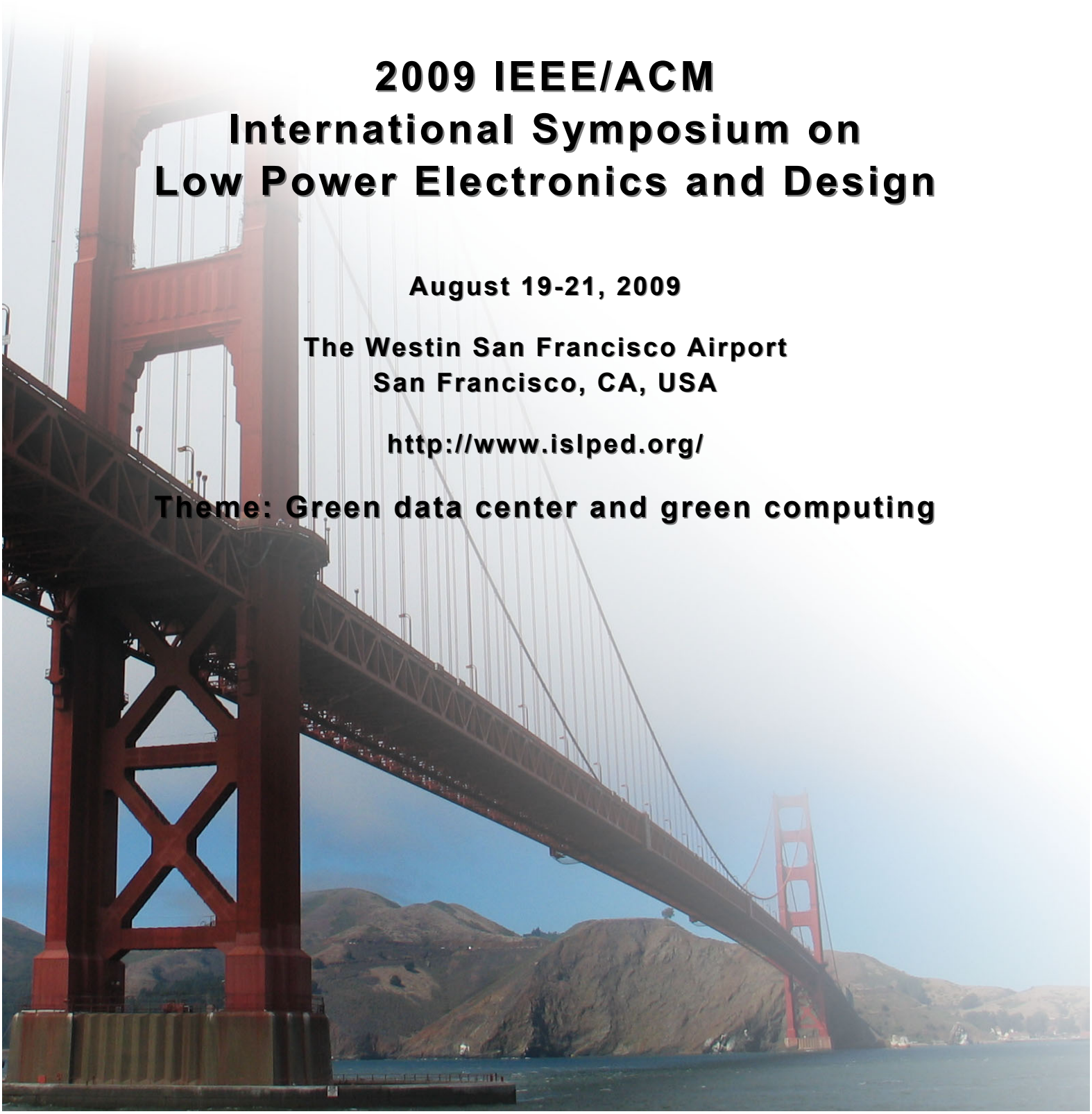
2009 IEEE/ACM International Symposium on Low Power Electronics and Design

August 19-21, 2009

The Westin San Francisco Airport
San Francisco, CA, USA

http://www.islped.org/

Theme: Green data center and green computing



Message from the Chairs

Welcome to the 14th ACM/IEEE International Symposium on Low Power Electronics and Design!

The 2009 edition of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED) welcomes you to San Francisco, the liberal fog-city of million rainbows by the bay in California, USA.

On a par with this great location, a strong and diverse technical program features four exciting keynote talks from leaders in the field, two plenary special sessions in line with our symposium theme on Green Data Centers and Computing, a technical panel on SoC Power management, and four informative half-day embedded tutorials scheduled for the last day of the symposium. New for this year's ISLPED green computing has been identified as the symposium theme with an array of invited keynote speeches, special sessions and tutorials covering this theme.

Dr. Percy Gilbert, VP of Technology Development at IBM, will give a keynote on advances in process technology and IBM collaborative ecosystem for leadership power performance SOC designs on Wednesday. The Thursday keynote will be delivered by Dr. Kevin Zhang, director of advanced design and Intel Fellow, who will discuss the opportunities and challenges of circuit design in Nano-Scale CMOS era. We will have two keynote speeches on Friday by Dr. Mojy Chian, the senior VP of the newly formed Global Foundries and by Dr. Yankin Tanurhan, VP of engineering and design at VirageLogic. Dr. Mojy Chian and Dr. Yankin Tanurhan will give talks on the challenges of low-power design enablement for foundry technology offerings and various opportunities in the semiconductor industry for the IP suppliers. These keynotes talks cover the topic from foundry technology to IP design and will be interesting to see the speakers' perspectives on what are the demands of IP design from advanced technologies.

New for ISLPED 2009 is the introduction of a theme. This year's theme focuses on "green computing" toward which special sessions and tutorials are lined up. On Wednesday, we have a two-hour special session on green data centers including green data centers power management, integrated compute and packaging solutions, and more by Prof. Massoud Pedram, University of Southern California, Prof. Tom Wenisch, University of Michigan, Cullen Bash, principal scientist and research manager at Hewlett Packard Labs, and John Carter, manager of power-aware systems at IBM Austin Research Laboratory. The Thursday special session welcomes three speakers, Dr. Kiyoo Itoh, fellow of Hitach, Al Fazio, fellow and director of Memory Technology Development at Intel, and Prof. Suman Datta form Pennsylvania State University covering green computing topics including low power and future non-volatile memories, low voltage circuits and green transistors.

On Thursday, a panel is scheduled on SoC Power Management and its controversial topics. This panel will be moderated by Brian Fuller who is an editor and consultant. We have four panelists including Sandeep Mirchandani from Broadcom, Sanjeev Das from NXP, Ran Avinun from Cadence, and Camille Kokozaki of IDT.

The four embedded tutorials on Friday are organized around major themes of (1) semiconductor technologies for green computing, and (2) system design issues with emerging technologies. Prof. Kaushik Roy of Purdue University will introduce ultra low voltage CMOS. Prof. Suman Datta of Pennsylvania State University and Prof. Vijay Narayanan of Pennsylvania State University will cover green transistors to green architectures. Prof. Vijay Raghunathan of Purdue University will introduce the topic of self-powered embedded systems and Dr. Norm Jouppi, fellow of HP Labs and Prof. Yuan Xie of Pennsylvania State University will discuss emerging technologies and their impact on system design.

We have a very exciting technical program in ISLPED 2009. Out of 208 paper submissions that we received, 72 strong technical papers were accepted for presentation in paper or poster sessions, yielding an acceptance rate of 25% for regular and short papers (52 papers), or 35% including the additional 20 posters. Topics range from low power technology, circuits, and memory; low voltage analog and RF design; power aware design and tools; power efficient architecture techniques; and system and application level power optimization. The program is organized into eleven technical sessions featuring long (30 min) and short (20 min) paper presentations, as well as one interactive poster session that will provide an additional venue for authors and symposium attendees to interact in an informal setting. Following the tradition ISLPED includes industry sessions and exhibits featuring tools and methodologies from leading vendors of low power or power-aware design tools. Winning entries to the annual Student Low Power Design Contest will also be featured in a separate technical session in ISLPED.

Such a rich and strong program would have not been possible without the help of an outstanding Technical Program Committee who has worked for weeks reviewing and on-site TPC meeting to select the best papers. Our many thanks go to the 2009 ISLPED officers who have made everything work like clockwork: Subramani Kengeri and Hamid Mahmoodi, Local Arrangements; Yuan Xie, Treasurer; Qing Wu and Vasantha Erraguntla, Exhibits; Yu Cao and Chris Hyung-il Kim, Design Contest; Farzan Fallah and Vijay Raghunathan, Publicity, Yung-Hsiang Lu, Web; Suman Datta, Panel; and Partha Ranganathan, Special Session.

ISLPED is grateful for the support it has received from ACM Special Interest Group on Design Automation and the IEEE Circuits and Systems Society. ISLPED also receives technical co-sponsorship from the IEEE Solid State Circuits and the IEEE Electron Devices Societies and is thankful for the generous financial support from Intel, Cadence, Mentor Graphics, and IBM.

We hope you will find ISLPED an exciting venue for interacting with fellow researchers in the field!

Jörg Henkel and Ali Keshavarzi — *General Co-chairs*

Naehyuck Chang and Tahir Ghani — *Technical Program Co-chairs*

Technical Program

	Wednesday, August 19, 2009	
08:00- 08:30	**Breakfast** **ABWS Foyer**	
08:30- 08:45	**Welcome by General and Program Co-Chairs** **ABWS Ballroom** General Co-Chairs: Ali Keshavarzi, TSMC and Joerg Henkel, Univ. of Karlsruhe Program Co-Chairs: Naehyuck Chang, Seoul National Univ. and Tahir Ghani, Intel Corp.	
08:45- 09:45	**Keynote Talk 1** **ABWS Ballroom** Chair: Ali Keshavarzi, TSMC	
	Percy V. Gilbert, VP of Technology Development, IBM Advances in Process Technology & IBM Collaborative Ecosystem for Leadership Power Performance SOC Designs	
09:45- 10:00	Break ABWS Foyer	
10:00- 12:00	**Sub-threshold circuits (1.1.1)** **ABW Ballroom** Chair: Nam Sung Kim, Univ. of Wisconsin-Madison Co-Chair: Radu Zlatanovici, Cadence	**Managing process variability (2.1.1)** **Sequoia Ballroom** Chair: Saibal Mukhopadhyay, Georgia Tech. Co-Chair: Vishwani Agrawal, Auburn Univ.
	Nanometer MOSFET Effects on the Minimum-Energy Point of 45nm Subthreshold Logic David Bol, Univ. Catholique de Louvain Dina Kamel, Univ. Catholique de Louvain Denis Flandre, Univ. Catholique de Louvain Jean-Didier Legat, Univ. Catholique de Louvain	ß Hybrid Logical-Statistical Simulation with Thermal and IR-Drop Mapping for Degradation and Variation Prediction Domenik Helms, OFFIS research Kai Hylla, OFFIS research Wolfgang Nebel, University Oldenburg
	Design and Analysis of Ultra-Thin-Body SOI Based Subthreshold SRAM Vita Pi-Ho Hu, National Chiao Tung Univ. Yu-Sheng Wu, National Chiao Tung Univ. Ming-Long Fan, National Chiao Tung Univ. Pin Su, National Chiao Tung Univ. Ching-Te Chuang, National Chiao Tung Univ.	ß Variation-Aware Supply Voltage Assignment for Minimizing Circuit Degradation and Leakage Xiaoming Chen, Tsinghua Univ. Yu Wang, Tsinghua Univ. Yu Cao, Arizona State Univ. Yuchun Ma, Tsinghua Univ. Huazhong Yang, Tsinghua Univ.
	Slew-Aware Clock Tree Design for Reliable Subthreshold Circuits **[s]** Jeremy R. Tolbert, Georgia Institute of Tech. Xin Zhao, Georgia Institute of Tech. Sung-Kyu Lim, Georgia Institute of Tech. Saibal Mukhopadhyay, Georgia Institute of Tech.	A Centralized Supply Voltage and Local Body Bias-Based Compensation Approach to Mitigate Within-die Process Variation **[s]** Amlan Ghosh, Univ. of Utah Rahul M. Rao, IBM Richard B. Brown, Univ. of Utah
	Technology Flavor Selection and Adaptive Techniques for Timing-Constrained 45nm Subthreshold Circuits **[s]** David Bol, Univ. Catholique de Louvain Denis Flandre, Univ. Catholique de Louvain Jean-Didier Legat, Univ. Catholique de Louvain	Tuning-Friendly Body Bias Clustering for Compensating Random Variability in Subthreshold Circuits **[s]** Koichi Hamamoto, Osaka Univ. Masanori Hashimoto, Osaka Univ. Yukio Mitsuyama, Osaka Univ. Takao Onoye, Osaka Univ.

	Serial Sub-threshold Circuits for Ultra-Low-Power Systems **[s]** Sudhanshu Khanna, Univ. of Virginia Benton H. Calhoun, Univ. of Virginia	Statistical Static Timing Analysis Considering Leakage Variability in Power Gated Designs **[s]** Michael J. Anderson, Univ. of Wisconsin-Madison Azadeh Davoodi, Univ. of Wisconsin-Madison Jungseob Lee, Univ. of Wisconsin-Madison Abhishek Sinkar, Univ. of Wisconsin-Madison Nam Sung Kim, Univ. of Wisconsin-Madison
12:00- 13:00	**Lunch** **Bayshore Ballroom**	
13:00- 15:00	**Energy-efficient analog subsystems (1.3)** **ABW Ballroom** Chair: Thomas Szepesi, PMChip Co-Chair: Suhwan Kim, Seoul National Univ.	**Dynamic thermal management (2.2.1)** **Sequoia Ballroom** Chair: Gilberto Contreras, NVIDIA Co-Cair: Li Shang, Univ. of Colorado at Boulder
	A Low Power High Noise Immunity Boost DC-DC Converter Using the Differential Difference Amplifiers Jiwei Fan, NC State Univ. Xin Zhou, NC State Univ. Liyu Yang, NC State Univ. Alex Huang, NC State Univ.	PPT: Joint Performance/Power/Thermal Management of DRAM Memory for Multi-Core Systems Chung-Hsiang Lin, National Taiwan University Chia-Lin Yang, National Taiwan University Ku-Jei King, IBM
	A Single Inductor Dual Input Dual Output DC-DC Converter with Hybrid Supplies for Solar Energy Harvesting Applications Hui Shao, Hong Kong Univ. of Science and Tech. Chi-Ying Tsui, Hong Kong Univ. of Science and Tech. Wing-Hung Ki, Hong Kong Univ. of Science and Tech.	Predict and Act: Dynamic Thermal Management for Multi-Core Processors Raid Z. Ayoub, UC San Diego Tajana S. Rosing, UC San Diego
	A CMOS Low Power Current-Mode Polyphase Filter **[s]** Hussain Alzaher, King Fahd University of Petroleum & Minerals Noman Tasadduq, King Fahd University of Petroleum & Minerals	Online Work Maximization under a Peak Temperature Constraint Thidapat Chantem, University of Notre Dame X. Sharon Hu, University of Notre Dame Robert P. Dick, University of Michigan
	Improvement of Power Efficiency in Switched Capacitor DC-DC Converter by Shoot-through Current Elimination **[s]** Ratna Kumar P. V, IIT-Kharagpur Kaushik Bhattacharyya, IIT-Kharagpur Tamal Das, IIT-Kharagpur Pradip Mandal, IIT-Kharagpur	Dynamic Thermal Management using Thin-Film Thermoelectric Cooling Pedro Chaparro, Intel Jose Gonzalez, Intel Qiong Cai, Intel Greg Chrysler, Intel
	Inductor Design of 20-V Boost Converter for Low Power 3D Solid State Drive with NAND Flash Memories **[s]** Tadashi Yasufuku, Univ. of Tokyo Koichi Ishida, Univ. of Tokyo Shinji Miyamoto, Toshiba Hiroto Nakai, Toshiba Makoto Takamiya, Univ. of Tokyo Takayasu Sakurai, Univ. of Tokyo Ken Takeuchi, Univ. of Tokyo	
15:00- 15:15	Break ABWS Foyer	
15:15- 16:45	**Design Contest** **ABW Ballroom** Co-Chair: Kevin (Yu) Cao, Arizona State Univ. Co-Chair: Chris Hyung-il Kim, Univ. of Minnesota	**Power optimization (2.1.2)** **Sequoia Ballroom** Chair: Renu Mehra, Synopsys Co-Chair: Vivek Tiwari, Intel Corp.
	A 2.6 μW Sub-Threshold Mixed-Signal ECG SoC Steven C. Jocke, Univ. of Virginia	Frequency and Yield Optimization using Power Gates in Power-Constrained Designs

	Jonathan F. Bolus, Univ. of Virginia Stuart N. Wooters, Univ. of Virginia Travis N. Blalock, Univ. of Virginia Benton H. Calhoun, Univ. of Virginia	Nam Sung Kim, University of Wisconsin-Madison Jun Seomun, KAIST Abhishek Sinkar, University of Wisconsin-Madison Jungseob Lee, University of Wisconsin-Madison Tae Hee Han, Sungkyunkwan University Ken Choi, Illinois Inst. of Tech. Youngsoo Shin, KAIST
	A 0.9V, 65nm Logic-compatible Embedded DRAM with 1ms Data Retention Time and 53% Less Static Power than a Power-Gated SRAM Ki Chul Chun, Univ. of Minnesota Pulkit Jain, Univ. of Minnesota Chris H. Kim, Univ. of Minnesota	NBTI-Aware Power Gating for Concurrent Leakage and Aging Optimization **[s]** Andrea Calimera, Politecnico di Torino Enrico Macii, Politecnico di Torino Massimo Poncino, Politecnico di Torino
		The Opportunity Cost of Low Power Design: A Case Study in Circuit Tuning **[s]** Matthew M. Ziegler, IBM Victor V. Zyuban, IBM George D. Gristede, IBM Milena Vratonjic, UC Davis Joshua Friedrich, IBM
		Behavior-Level Observability Don't-Cares and Application to Low-Power Behavioral Synthesis **[s]** Jason Cong, UCLA Bin Liu, UCLA Zhiru Zhang, AutoESL Design Technologies, Inc
16:45- 17:00	Break ABWS Foyer	
17:00- 19:00	**Special Session 1 – Green Data Centers** **ABWS Ballroom** Chair: Partha Ranganathan, Hewlett Packard Labs Co-Chair: Subhasish Mitra, Stanford University	
	Ehsan Pakbaznia, Massoud Pedram, Univ. of Southern California Minimizing Data Center Cooling and Server Power Costs	
	Tom Wenisch, Univ. of Michigan Thinking Outside the Box: Power Management at the System Level & Beyond	
	John Carter, IBM Austin Research A Look Inside IBM's Green Data Center Research	
	Cullen Bash, Hewlett Packard Sustainable IT Ecosystems and Data Centers	
19:00- 21:00	**Wine and cheese reception** **Bayshore Ballroom**	

	Thursday, August 20, 2009	
08:00- 08:30	**Breakfast** **ABWS Foyer**	
08:30- 09:30	**Keynote Talk 2** **ABWS Ballroom** Chair: Vivek De, Intel Corp.	
	Kevin Zhang, Fellow, Intel Circuit Design in Nano-Scale CMOS Era: Opportunities & Challenges	
09:30- 09:45	Break ABWS Foyer	
09:45- 11:45	**Micro-architecture techniques (1.2.1)** **ABW Ballroom** Chair: Farhad Mehdipour, Kyushu Univ. Co-Chair: Alper Buyuktosunoglu, IBM	**Variation-aware and adaptive power management (2.2.2)** **Sequoia Ballroom** Chair: Sharon Hu, Univ. of Notre Dame Co-Chair: Elaheh Bozorgzadeh, UC Irvine
	ß Way-Tagged Cache: An Energy-Efficient L2 Cache Architecture under Write-Through Policy Jianwei Dai, University of Connecticut Lei Wang, University of Connecticut	Analyzing Potential Power Reduction with Adaptive Voltage Positioning Optimized for Multicore Processors Abhishek Sinkar, Univ. of Wisconsin - Madison Nam Sung Kim, Univ. of Wisconsin - Madison
	Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches Mrinmoy Ghosh, Georgia Institute of Tech. and ARM Emre Ozer, ARM Simon Ford, ARM Stuart Biles, ARM Hsien-Hsin S. Lee, Georgia Institute of Tech.	Significance Driven Computation: A Voltage-Scalable, Variation-Aware, Quality-Tuning Motion Estimator Debabrata Mohapatra, Purdue University Georgios Karakonstantis, Purdue University Kaushik Roy, Purdue University
	Energy-Efficient Renaming with Register Versioning **[s]** Hui Zeng, SUNY, Binghamton Ju-Young Jung, SUNY, Binghamton Kanad Ghose, SUNY, Binghamton Dimitry Ponomarev, SUNY, Binghamton	Optimizing Total Power of Many-Core Processors Considering Voltage Scaling Limit and Process Variations Jungseob Lee, University of Wisconsin-Madison Nam Sung Kim, University of Wisconsin-Madison
	Cooperative Shared Resource Access Control for Low-Power Chip Multiprocessors **[s]** Noriko Takagi , University of Tokyo Hiroshi Sasaki , University of Tokyo Masaaki Kondo, University of Electro-Communications Hiroshi Nakamura, University of Tokyo	Integrating Dynamic Voltage/Frequency Scaling and Adaptive Body Biasing using Test-time Voltage Selection Alyssa Bonnoit, Carnegie Mellon University Sebastian Herbert, Carnegie Mellon University Diana Marculescu, Carnegie Mellon University Lawrence Pileggi, Carnegie Mellon University
	An Energy-Efficient Checkpointing Mechanism For Out Of Order Commit Processor **[s]** Hui Zeng, SUNY, Binghamton Matt T. Yourst, SUNY, Binghamton Kanad Ghose, SUNY, Binghamton	
11:45- 12:45	**Lunch** **Bayshore Ballroom**	
12:45- 14:45	**Digital low-power potpourri (1.1.2)** **ABW Ballroom** Chair: David Wentzloff, Univ. of Michigan Co-Chair: Borivoje Nikolic, UC Berkeley	**Energy-aware client-server computing (2.3.1)** **Sequoia Ballroom** Chair: Ken Choi, Illinois Institute of Tech. Co-Chair: Brarry Pangrle, Mentor Graphics
	Pulse Width Modulation for Reduced Peak Power Full-Swing On-Chip Interconnect Mackenzie R. Scott, UC Davis Rajeevan Amirtharajah, UC Davis	ß vGreen: A System for Energy Efficient Computing in Virtualized Environments Gaurav Dhiman, UC San Diego Giacomo Marchetti, UC San Diego Tajana Rosing, UC San Diego

	ß Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs) Daeyeon Kim, University of Michigan Yoonmyung Lee, University of Michigan Jin Cai, IBM Isaac Lauer, IBM Leland Chang, IBM Steven J. Koester, IBM Dennis Sylvester, University of Michigan David Blaauw, University of Michigan	Near optimal battery-aware energy management Sushu Zhang, Arizona State University Karam S. Chatha, Arizona State University Goran Konjevod, Arizona State University
	A 45nm CMOS 0.35V-Optimized Standard Cell Library for Ultra-Low Power Applications **[s]** Fady Abouzeid, STMicroelectronics Sylvain Clerc, STMicroelectronics Fabian Firmin, STMicroelectronics Marc Renaudin, Tiempo SAS Gilles Sicard, TIMA Laboratory	Transaction-Based Adaptive Dynamic Voltage Scaling for Interactive Applications **[s]** Xia Zhao, Peking University Yao Guo, Peking University Xiangqun Chen, Peking University
	A Low Power 3D Integrated FFT Engine Using Hypercube Memory Division **[s]** Thorlindur Thorolfsson, NCSU Nariman Moezzi Madani, NCSU Paul D. Franzon, NCSU	Tracking the Power in an Enterprise Decision Support System **[s]** Justin Meza, HP Labs Mehul Shah, HP Labs Parthasarathy Ranganathan, HP Labs Mike Fitzner, HP BCS Judson Veazey, HP BCS
	Data Manipulation Techniques to Reduce Phase Change Memory Write Energy **[s]** Wei Xu, Rensselaer Polytechnic Institute Jibang Liu, Rensselaer Polytechnic Institute Tong Zhang, Rensselaer Polytechnic Institute	Ranking Servers based on Energy Savings for Computation Offloading **[s]** Karthik Kumar, Purdue University Yamini Nimmagadda, Purdue University Yung-Hsiang Lu, Purdue University
14:45- 15:00	Break ABWS Foyer	
15:00- 16:30	**Special Session 2 – Green Computing** **ABWS Ballroom** Chair: Eddie Pettis, Google	
	Kiyoo Itoh, Fellow, Hitachi Leakage- and Variability-Conscious Circuit Designs for the 0.5-V Nanoscale CMOS Era	
	Al Fazio, Fellow, Intel Non Volatile Memories to Enable System Power Scaling	
	Suman Datta, Pennsylvania State Univ. Low Voltage Tunnel Transistor Architecture and its Viability for Energy Efficient Logic Applications	
16:30- 16:45	Break ABWS Foyer	
16:45- 18:00	**Poster Session** **ABWS Ballroom** Chair: Hamid Mahmoodi, San Francisco State Univ. Co-chair: Jinfeng Liu, Synopsys	
	Cross-Over Current Suppressing Latch Compared to State-of-the-Art for Low-Power Low-Frequency Applications with Resonant Clocking Flavio Carbognani, ETH Zurich Luca Henzen, ETH Zurich	Reducing the Leakage and Timing Variability of 2D ICs Using 3D ICs Sherief Reda, Brown University Aung Si, Brown University Iris Bahar, Brown University
	An optimization strategy for low energy and high performance for the on-chip interconnect signaling Ge Chen, University of New South Wales Saeid Nooshabadi, Gwang Inst. of Science and Tech. Steven Duvall, University of New South Wales	A High-Performance Low-Power Nanophotonic On-Chip Network Zheng Li, Tsinghua University Jie Wu, Tsinghua University Li Shang, University of Colorado at Boulder Alan R. Mickelson, University of Colorado at Boulder Manish Vachharajani, University of Colorado at Boulder

	An optimization strategy for low energy and high performance for the on-chip interconnect signaling Ge Chen, University of New South Wales Saeid Nooshabadi, Gwang Inst. of Science and Tech. Steven Duvall, University of New South Wales	Dejan Filipovic, University of Colorado at Boulder Wounjhang Park, University of Colorado at Boulder Yihe Sun, Tsinghua University
	Exploration of 3D Stacked L2 Cache Design for High Performance and Efficient Thermal Control Guangyu Sun, Pennsylvania State Univ. XiaoXia Wu, Pennsylvania State Univ. Yuan Xie, Pennsylvania State Univ.	Power-Management-Based Chien Search for Low Power BCH Decoder Shu-Yi Wong, University of Windsor Chunhong Chen, University of Windsor Q. M. Jonathan Wu, University of Windsor
	Low Power Robust Signal Processing Veera Papirla, Arizona State University Aarul Jain, Arizona State University Chaitali Chakrabarti, Arizona State University	Enabling Ultra Low Voltage System Operation by Tolerating On-Chip Cache Failures Amin Ansari, University of Michigan Shuguang Feng, University of Michigan Shantanu Gupta, University of Michigan Scott Mahlke, University of Michigan
	Design of Multi-Mode 4-Switch Buck-Boost Controller Lou Jiana, Zhejiang University Wu Xiaobo, Zhejiang University	Electromigration Study of Power Gated Grids AidaTodri, UC Santa Barbara Malgorzata Marek-Sadowska, UC Santa Barbara
	Software-Defined SIMO Step-Up/Down Power Converter with Adaptive Global/Local Power Allocation Scheme for DVS-Enabled Multicore Systems Feng Luo, University of Arizona Rajdeep Bondade, University of Arizona Dongsheng Ma, University of Arizona	A Novel 0.5V 15¼W 1.3MHz Temperature-Compensated Analog PWM-Controller for Switch-Mode Converters Dominic Maurath, IMTEK Charalambos Andreou, IMTEK Yiannos Manoli, IMTEK
	SOI, Interconnect, Package, and Mainboard Thermal Characterization Joseph Nayfach-Battilana, UC Santa Cruz Jose Renau, UC Santa Cruz	N-Version Temperature-Aware Scheduling and Binding Yousra Alkabani, Rice University Farinaz Koushanfar, Rice University Miodrag Potkonjak, UCLA
	Energy-Aware Instruction-Set Customization for Real-Time Embedded Multiprocessor Systems Seungrok Jung, Samsung Jungsoo Kim, KAIST Sangkwon Na, KAIST Chong-Min Kyung, KAIST	Power-Saving Color Transformation of Mobile Graphical User Interfaces on OLED-based Displays Mian Dong, Rice University Yung-Seok K. Choi, Rice University Lin Zhong, Rice University
	An Energy-Delay Efficient 2-Level Data Cache Architecture for Embedded System Jongmin Lee, KAIST Soontae Kim, KAIST	Experimental Analysis of Sequence Dependence on Energy Saving for Error Tolerant Image Processing Se H. Kim, Georgia Institute of Technology Saibal Mukhopadhyay, Georgia Institute of Technology Wayne Wolf, Georgia Institute of Technology
	A Programmable Implementation of Neural Signal Processing on a Smartdust for Brain-Computer Interfaces Yuwen Sun, University of Pittsburgh Shimeng Huang, University of Pittsburgh Joseph Oresko, University of Pittsburgh John Krais, University of Pittsburgh Allen C. Cheng, University of Pittsburgh	An Experimental Validation of System Level Design Space Exploration Methodology for Energy Efficient Sensor Nodes Sonali Chouhan, Indian Institute of Technology Delhi M. Balakrishnan, Indian Institute of Technology Delhi Ranjan Bose, Indian Institute of Technology Delhi
18:00-19:00	**Panel** **ABWS Ballroom** Chair: Suman Datta, Pennsylvania State Univ.	
	It is All About Power Analysis, Exploration and Trade-offs Organizer: Soheil Modirzadeh, Cadence Moderator: Brian Fuller, Editor and Consultant Panelists: Sandeep Mirchandani, Broadcom / Sanjeev Das, NXP / Ran Avinun, Cadence / Camille Kokozaki, IDT / Jon McDonald, Mentor Graphics	

19:00- 22:00	**Banquet** **Shalizar Restaurant**

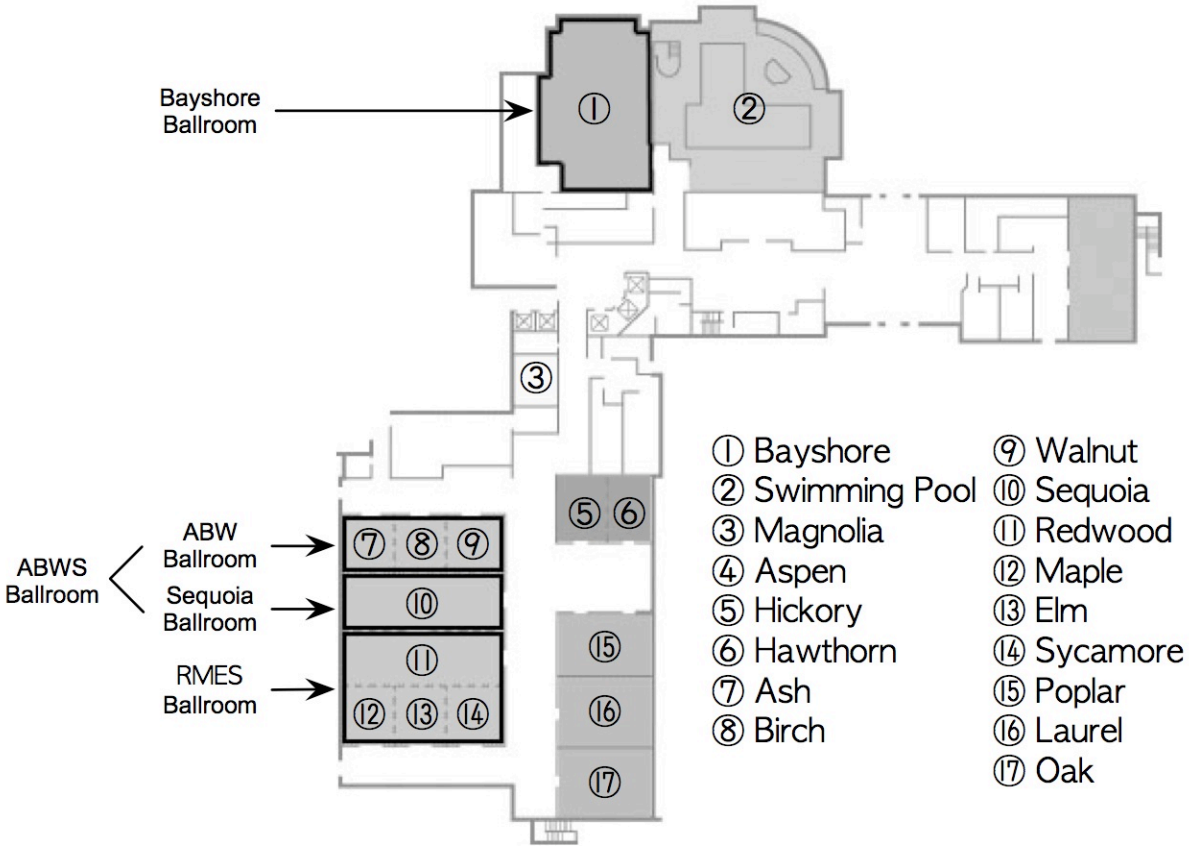
	Friday, August 21, 2009	
08:00- 08:30	**Breakfast** **ABWS Foyer**	
08:30- 09:15	**Keynote Talk 3** **ABWS Ballroom** Chair: Subramani Kengeri, GLOBALFOUNDRIES	
	Mojy Chian, Senior VP, GLOBALFOUNDRIES Challenges and Opportunities in Low-Power Design Enablement	
09:15- 10:00	**Keynote Talk 4** **ABWS Ballroom** Chair: Sreedhar Natarajan, TSMC	
	Yankin Tanurhan, VP of Engineering and Design, VirageLogic Dealing with Disaggregation in Ever-changing World of Semiconductors	
10:00- 10:15	Break ABWS Foyer	
10:15- 12:15	**Low-power platforms and circuits (1.2.2)** **ABW Ballroom** Chair: Hiroshi Sasaki, Tokyo Univ. Co-Chair: Lawrence Clark, Arizona State Univ.	**Energy-efficient wireless systems (2.3.2)** **Sequoia Ballroom** Chair: Tajana Simunic Rosing, UC San Diego Co-Chair: Vijay Raghunathan, Purdue Univ.
	A 60fps 496mW Multi-Object Recognition Processor with Workload-Aware Dynamic Power Management **[s]** Joo-Young Kim, KAIST Seungjin Lee, KAIST Jinwook Oh, KAIST Minsu Kim, KAIST Hoi-Jun Yoo, KAIST	Adaptive RF Chain Management for Energy-Efficient Spatial-Multiplexing MIMO Transmission Hang Yu, Rice University Lin Zhong, Rice University Ashutosh Sabharwal, Rice University
	The Design of a Bloom Filter Hardware Accelerator for Ultra Low Power Systems **[s]** Michael J. Lyons, Harvard University David Brooks, Harvard University	Remote Progressive Firmware Update for Flash-Based Networked Embedded Systems Jinsik Kim, University of California, Irvine Pai H. Chou, University of California, Irvine
	Dynamic Power Gating with Quality Guarantees **[s]** Anita Lungu, Duke University Pradip Bose, IBM Alper Buyuktosunoglu, IBM Daniel J. Sorin, Duke University	Power Management in Energy Harvesting Embedded Systems with Discrete Service Levels Clemens Moser, ETH Zurich Jian-Jia Chen, ETH Zurich Lothar Thiele, ETH Zurich
	End-to-End Validation of Architectural Power Models **[s]** Madhu S. S. Govindan, , Univ. of Texas at Austin Stephen W. Keckler, Univ. of Texas at Austin Doug Burger, Microsoft Research	Energy Efficient Sampling for Event Detection in Wireless Sensor Networks Zainul Charbiwala, UCLA Younghun Kim, UCLA Sadaf Zahedi, UCLA Jonathan Friedman, UCLA Mani Srivastava, UCLA
	Low Power Fast and Dense Longest Prefix Match Content Addressable Memory for IP Routers **[s]** Satendra Kumar Maurya, Arizona State University Lawrence T. Clark, Arizona State University	

	MicroFix: Exploiting Path-grained Timing Adaptability for Improving Power-Performance Efficiency **[s]** Guihai Yan, ICT, Chinese Academy of Sciences Yinhe Han, ICT, Chinese Academy of Sciences Hui Liu, ICT, Chinese Academy of Sciences Xiaoyao Liang, NVIDIA Xiaowei Li, ICT, Chinese Academy of Sciences	
12:15- 13:00	**Lunch** **RMES Ballroom**	
13:00- 14:00	**Embedded Tutorial 1** **ABW Ballroom** Chair: Chris Hyung-il Kim, Univ. of Minnesota	**Embedded Tutorial 2** **Sequoia Ballroom** Chair: Yung-Hsiang Lu, Purdue Univ.
	Ultra Low Voltage CMOS Kaushik Roy, Purdue University	**Emerging Technologies and Their Impact on System Design** Yuan Xie, Pennsylvania State Univ.
14:00- 15:00	**Embedded Tutorial 3** **ABW Ballroom** Chair: Koji Inoue, Kyushu Univ.	**Embedded Tutorial 4** **Sequoia Ballroom** Chair: Chia-Lin Yang, National Taiwan Univ.
	Green Transistors to Green Architectures Suman Datta, Pennsylvania State Univ. Vijay Narayanan, Pennsylvania State Univ.	**Green at the Micro-Scale: Towards Self-Powered Embedded Systems** Vijay Raghunathan, Purdue Univ.
15:15	**Closing Remarks** **ABWS Ballroom**	

Conference Hotel Layout

The Westin Hotel San Francisco Airport
(1 Old Bayshore Highway · Millbrae, California 94030)

Lobby Level



Banquet Event

Thu, Aug 20th, 7-10pm

Shalizar Restaurant
300 El Camino Real, Belmont, CA 94002
650-596-9000

http://www.shalizaar.com

Come and enjoy an evening of Persian food and music!!!

Shuttle Transportation to Event

Shuttle busses will be leaving from the hotel between 7pm and 7:30pm. Please catch the busses at the hotel entrance during this time. The shuttle busses will bring attendees back to the hotel at 10pm.

If you choose to drive to the restaurant, parking space is available at the restaurant. It is a 15 minute drive from the hotel (see the restaurant address above or map on the next page).

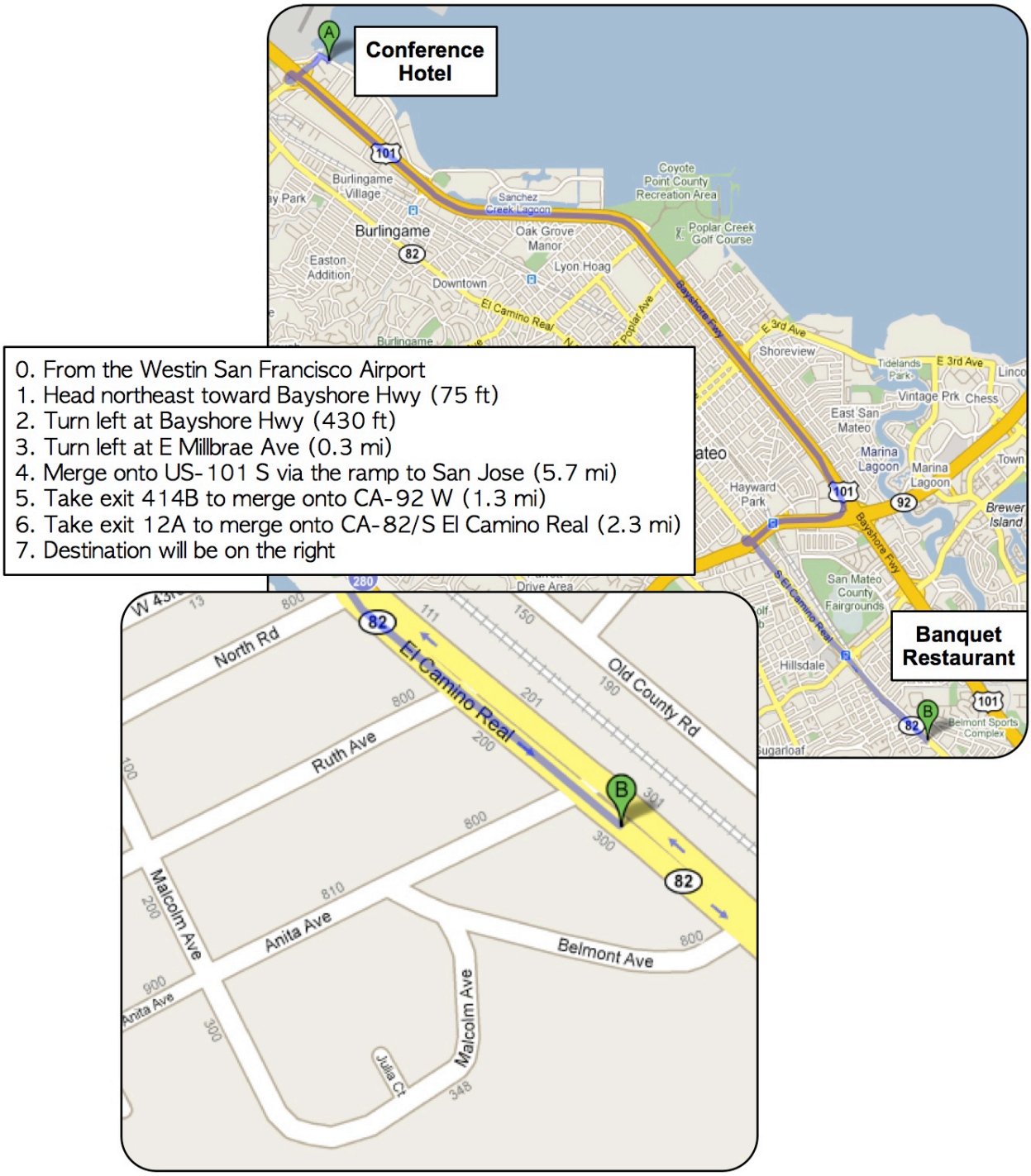
Conference registration covers one admission to the banquet event. If you would like to bring a partner/friend, limited additional banquet tickets are available for sale at the registration desk ($60/person). Please bring your conference badge or additional ticket for admission and complementary wine.

Private Vehicle Transportation to Event

The restaurant Shalizaar has a parking lot for 34 vehicles and there is no overflow parking lot. You may park your vehicle at the restaurant parking lot. However, parking is on the first-come-first-serve basis and if the parking lot is full, you should look for street parking. Please ask to the restaurant for more details.

Banquet Restaurant Map

Shalizar Restaurant
300 El Camino Real, Belmont, CA 94002



(Maps and driving direction from map.google.com)

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