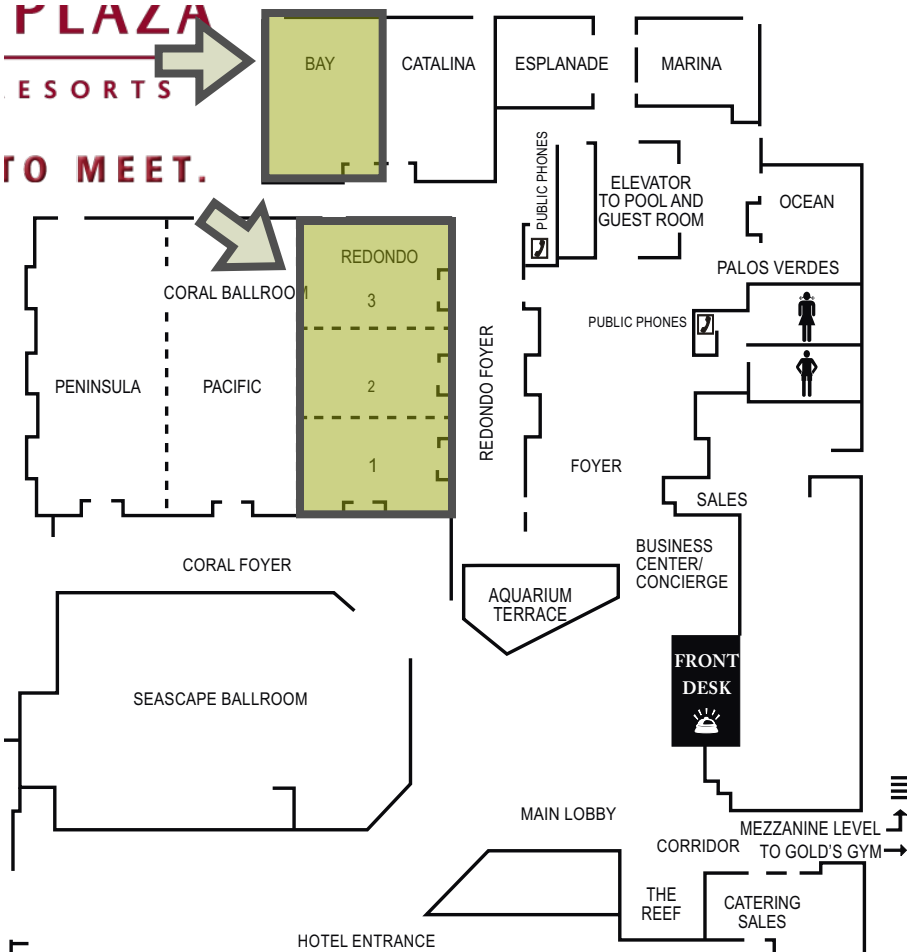


PLAZA

RESORTS

TO MEET.



(Advance Program as of July 16, 2012)

### MEETING ROOMS

The meeting rooms are Bay Room and Redondo Room. The plenary sessions are held in Redondo Room.

# ISLPED '12

## CROWNE PLAZA HOTEL REDONDO BEACH, CA

JULY 30-AUG. 1, 2012

(RECEPTION SUNDAY EVENING)

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# ISLPED 2012

## Program at a Glance

SUNDAY, JULY 29, 2012

TIME	ROOM 1	ROOM 2
18:00	Reception	

MONDAY, JULY 30, 2012

TIME	ROOM 1	ROOM 2
7:00	Breakfast	
8:00	Chairs' Welcome	
8:30	Keynote by Pradip Bose, IBM "Energy Secure Computing"	
9:30	Break	
10:00	Session 1: Circuits in Emerging Techniques	Session 2: Tools for Physical Design and Architecture Simulation
11:30	Lunch	
13:00	Session 3: Caches, Memories, and Interconnect	Session 4: Industry FOCUS Session on Low Power Design
15:00	Break	
15:30	Session 5: Low Power SRAM	Session 6: System Level Power Optimization
17:00	Session 7: Panel - Going Green Across Communication and Storage Subsystems	Session 8: Low Power Design and Validation Methodologies
18:30	(free activity)	

TUESDAY, JULY 31, 2012

TIME	ROOM 1	ROOM 2
7:00	Breakfast	
8:00	Keynote by Kaushik Roy, Purdue U. "Spin as State Variable for Computation: Prospects and Perspectives"	
9:00	Break	
9:30	Session 9: Digital Techniques	Session 10: Energy Efficiency and Non-Volatile Memories
11:30	Poster Session	
12:00	Lunch	
13:30	Session 11: Innovations in Low Power Analog	Session 12: Software-Driven Techniques for Energy Efficiency in Embedded Multi-Core Systems
15:30	Break	
16:00	Design Contest	Embedded Tutorial
17:30	Industry Reception	
19:00	Social Event - Banquet	

WEDNESDAY, AUGUST 1, 2012

TIME	ROOM 1	ROOM 2
7:30	Breakfast	
8:30	Keynote by Uming Ko, MediaTek USA, "Ultra-Low Power Challenges for the Next Generation ASIC"	
9:30	Break	
10:00	Session 13: Processor Design and Implementation	Session 14: Memory Management and Scheduling
12:00	Closing	

# Monday, July 30, 2012 (1/2)

TIME	BAY ROOM	REDONDO ROOM
7:00	<b>Breakfast</b>	
8:00	<b>Chairs' Welcome</b> (Bay Room)	
8:30	<b>Keynote: Energy Secure Computing</b> - Speaker: Pradip Bose, IBM Chair: Massimo Poncino, Politecnico di Torino	
9:30	<b>Break</b>	
10:00 - 11:30	<b>Session 1: Circuits in Emerging Techniques</b> Chair: Kangho Lee (Qualcomm), Co-Chair: Jae-Joon Kim (IBM)	<b>Session 2: Tools for Physical Design and Architecture Simulation</b> Chair: Houman Homayoun (George Mason U)
10:00	★ <i>Write-Optimized Reliable Design of STT MRAM</i> Yusung Kim, Sumeet Gupta, Sang Phill Park, Georgios Panagopoulos, Kaushik Roy (Purdue U)	<i>Practically Scalable Floorplanning with Voltage Island Generation</i> Song Chen, Xiaolin Zhang, Takeshi Yoshimura (Waseda U)
10:30	<i>High-Performance Low-Energy STT MRAM Based on Balanced Write Scheme</i> Dongsoo Lee, Sumeet Gupta, Kaushik Roy (Purdue U)	★ <i>TSV Array Utilization in Low-Power 3D Clock Network Design</i> Xin Zhao, Sung Kyu Lim (Georgia Institute of Technology)
11:00	<i>Design Benchmarking to 7nm with FinFET Predictive Technology Models</i> Saurabh Sinha, Brian Cline, Greg Yeric, Vikas Chandra (ARM); Yu Cao (Arizona State U)	<i>Thermal-Aware Sampling in Architectural Simulation</i> Ehsan K. Ardestani, Elnaz Ebrahimi, Gabriel Southern, Jose Renau (UC Santa Cruz)
11:30	<b>Lunch</b>	
13:00 - 15:00	<b>Session 3: Caches, Memories, and Interconnect</b> Chair: Saurabh Sinha (ARM), Co-Chair: Xiangyu Dong (Qualcomm)	<b>Session 4: Industry Focus Session on Low Power Design</b> Chair: Clive Bittlestone (Texas Instruments)

TIME	BAY ROOM	REDONDO ROOM
13:00	★ <i>ER: Elastic RESET for Low Power and Long Endurance MLC based Phase Change Memory</i> Lei Jiang, Youtao Zhang, Jun Yang (U of Pittsburgh)	<i>Advances in Ultrabook™ Platform Power Management</i> Jim Kardach (Intel Corp.)
13:30	<i>A Dual-mode Architecture for Fast-switching STT-RAM</i> Zhenyu Sun, Hai (Helen) Li (Polytechnic Institute of New York U); Wenqing Wu (Qualcomm Inc)	<i>Commercial Low-Power EDA Tools: A Review</i> Renu Mehra (Synopsys)
14:00	<i>ASCIB: Adaptive Selection of Cache Indexing Bits for Removing Conflict Misses</i> Alberto Ros (Universidad de Murcia); Polychronis Xekalakis (Intel Labs Barcelona); Marcelo Cintra (The University of Edinburgh); Manuel E. Acacio, José M. García (Universidad de Murcia)	<i>An ARM perspective on Addressing Low-Power Energy-Efficient SoC Designs</i> David Flynn (ARM)
14:30	<i>Energy Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Systems</i> Jieming Yin, Pingqiang Zhou, Anup Holey, Sachin S. Sapatnekar, Antonia Zhai (U of Minnesota, Twin Cities)	<b>Panel:</b> Barry Pangrle (Mentor), Jim Kardach (Intel); Renu Mehra (Synopsys), David Flynn (ARM)
15:00	<b>Break</b>	
15:30 - 17:00	<b>Session 5: Low Power SRAM</b> Chair: Min Huang (Intel), Co-Chair: Sridhara (Texas Instruments)	<b>Session 6: System Level Power Optimization</b> Chair: Yung-Hsiang Lu (Purdue), Co-Chair: Ayse K. Coskun (Boston Univ.)

# Monday, July 30, 2012 (2/2)

TIME	BAY ROOM	REDONDO ROOM
15:30	<p><i>A 55nm 0.55V 6T SRAM with Variation-Tolerant Dual-Tracking Word-Line Under-Drive and Data-Aware Write-Assist</i> Yi-Wei Lin, Hao-I Yang, Geng-Cing Lin, Chi-Shin Chang, Ching-Te Chuang, Wei Hwang (National Chiao Tung U); Chia-Cheng Chen, Willis Shih, Huan-Shun Huang (Faraday Technology)</p>	<p><i>Power-aware Performance Increase via Core/Uncore Reinforcement Control for Chip-Multiprocessors</i> Da-Cheng Juan, Diana Marculescu (CMU)</p>
16:00	<p><i>A 40-nm 256-Kb Sub-10 pJ/Access 8T SRAM with Read Bitline Amplitude Limiting (RBAL) Scheme</i> Shusuke Yoshimoto, Masaharu Terada, Youhei Umeki, Shunsuke Okumura (Kobe University); Atsushi Kawasumi, Toshikazu Suzuki, Shinichi Moriwaki, Shinji Miyano (STARC); Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe U)</p>	<p><i>Power Conversion Efficiency Characterization and Optimization for Smartphones</i> Woojoo Lee, Yanzhi Wang (U of Southern California); Donghwa Shin, Naehyuck Chang (Seoul National U); Massoud Pedram (USC)</p>
16:30	<p><i>An Adaptive Write Word-Line Pulse Width and Voltage Modulation Architecture for Bit-Interleaved 8T SRAMs</i> Daeyeon Kim (U of Michigan); Vikas Chandra, Robert Aitken (ARM); David Blaauw, Dennis Sylvester (U of Michigan)</p>	<p><i>Dynamic Reconfiguration of Photovoltaic Energy Harvesting System in Hybrid Electric Vehicles</i> Yanzhi Wang, Xue Lin (USC); Naehyuck Chang (Seoul National U); Massoud Pedram (USC)</p> <p><i>Battery Management for Grid-connected PV Systems with a Battery</i> Sangyoung Park (SNU); Yanzhi Wang (USC); Younghyun Kim, Naehyuck Chang (SNU); Massoud Pedram (USC)</p>
17:00 - 18:30	<p><b>Session 7: Panel - Going Green Across Communication and Storage Subsystems</b> Session Chair: Ken Wagner (PMC-Sierra, Inc)</p>	<p><b>Session 8: Low Power Design and Validation Methodologies</b> Chair: Michael Orshansky (UT Austin)</p>

TIME	BAY ROOM	REDONDO ROOM
17:00	<p>Panelists: Martin St. Laurent (Qualcomm, USA) Robert Aitken (ARM, USA) Hugh Barrass (Cisco, USA) Randall Robinson (Rackforce Networks, Canada)</p>	<p><i>Modeling, Design and Cross-Layer Optimization of Polysilicon Solar Cell Based Micro-scale Energy Harvesting System</i> Elif Selin Mungan, Chao Lu, Kaushik Roy, Vijay Raghunathan (Purdue U)</p>
17:30	(panel continued)	<p><i>Static Low Power Verification Flow at Transistor Level for SoC Design</i> Jérôme Lescot, Vincent Bligny (STEricsson); Dina Medhat (Mentor Graphics); Didier Chollat-Namy (STEricsson); Ziyang Lu, Sophie Billy, Mark Hofmann (Mentor Graphics)</p>
18:00	(panel continued)	<p><i>CCP: Common Case Promotion for Improved Timing Error Resilience with Energy Efficiency</i> Lu Wan, Deming Chen (University of Illinois at Urbana-Champaign)</p> <p><i>Energy-Optimal Caches with Guaranteed Lifetime</i> Mirko Loghi (University di Udine); Haroon Mahmood, Andrea Calimera, Massimo Poncino, Enrico Macii (Politecnico di Torino)</p>
18:30	<b>(Free Activity)</b>	

# Tuesday, July 31, 2012 (1/3)

TIME	BAY ROOM	REDONDO ROOM
7:00	<b>Breakfast</b>	
8:00	<b>Keynote:</b> Spin as State Variable for Computation: Prospects and Perspectives Speaker: Kaushik Roy, Purdue University Chair: Naresh Shanbhag, UIUC	
9:00	<b>Break</b>	
9:30 - 11:30	<b>Session 9: Digital Techniques</b> Chair: Nikola Nedovic (Fujitsu), Co-Chair: Steven Bartling (Texas Instruments)	<b>Session 10: Energy Efficiency and Non-Volatile Memories</b> Chair: Elaheh Bozorgzadeh (UC Irvine), Co-Chair: John Sartori (UIUC)
9:30	<i>Register File Write Data Gating Techniques and Break-Even Analysis Model</i> Eric Donkoh, Teck Siong Ong, Yan Nee Too (Intel Corp); Patrick Chiang (Oregon State U)	<i>Improving Energy Efficiency of Write-Asymmetric Memories by Log Style Write</i> Guangyu Sun (Peking U.); Yaojun Zhang (UPitt), Yu Wang (Tsinghua U.); Yiran Chen (UPitt)
10:00	<i>A Low-Leakage Dynamic Register File with Unlocked Wordline and Sub-Segmentation for Improved Bitline Scalability</i> Eric Donkoh (Intel); Patrick Chiang (OSU)	<i>Process Variation Aware Data Management for STT-RAM Cache Design</i> Zhenyu Sun, Xiuyuan Bi, Hai (Helen) Li (Polytechnic Institute of New York U)
10:30	<i>A Fine-Grained Many V<sub>T</sub> Design Methodology for Ultra Low Voltage Operations</i> Mingoo Seok (Columbia U)	★ <i>TapeCache: A High Density, Energy Efficient Cache Based on Domain Wall Memory.</i> Rangharajan Venkatesan, Vivek Kozhikkottu (Purdue); Charles Augustine, Arijit Raychowdhury (Intel); Kaushik Roy, Anand Raghunathan (Purdue)
11:00	<i>A Programmable Resistive Power Grid for Post-Fabrication Flexibility and Energy Tradeoffs</i> Kyle Craig (U of Virginia & AMD), Yousef Shakhsher, Sudhanshu Khanna, Saad Arrabi, John Lach, Benton Calhoun (U of Virginia); Stephen Kosonocky (Advanced Micro Devices)	<i>A Software Approach for Combating Asymmetries of Non-Volatile Memories</i> Yong Li, Yiran Chen, Alex K. Jones (UPitt)
		<i>Design of Low Power 3D Hybrid Memory by Non-volatile CBRAM-Crossbar with Block-level Data-retention</i> Yuhao Wang, Chun Zhang, Hao Yu, Wei Zhang (Nanyang Tech. U)

★ best-paper candidate

TIME	BAY ROOM	REDONDO ROOM
11:30	<b>Poster Session</b> Chair: Antonia Zhai (Univ. of Minnesota), Co-Chair: Yuan Xie (Penn State Univ.)	
		<i>TAP: Token-Based Adaptive Power Gating.</i> Andrew Kahng, Seokhyeong Kang, Tajana Rosing, Richard Strong (UCSD)
		<i>Design Trade-Offs for High Density Cross-Point Resistive Memory.</i> Dimin Niu, Cong Xu (Penn State Univ.); Naveen Muralimanohar, Norman Jouppi (HP Labs); Yuan Xie (PSU)
		<i>Performance and Energy-Efficiency Improvement through Modified CPL in Organic Transistor Integrated Circuits.</i> Mingoo Seok (Columbia Univ.)
		<i>Optimal Power Switch Design for Dynamic Voltage Scaling from High Performance to Subthreshold Operation.</i> Kyle Craig, Yousef Shakhsher, Benton Calhoun (U. of Virginia)
		<i>BiN: A Buffer-in-NUCA Scheme for Accelerator-Rich CMPs.</i> Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Chunyue Liu, Glenn Reinman (UCLA)
		<i>Adopting TLB Index-based Tagging to Data Caches for Tag Energy Reduction.</i> Jongmin Lee, Soontae Kim (KAIST)
		<i>Static and Dynamic Co-Optimizations for Blocks Mapping in Hybrid Caches.</i> Yu-Ting Chen, Jason Cong, Hui Huang, Chunyue Liu, Raghu Prabhakar, Glenn Reinman (UCLA)
		<i>Design Space Exploration of Workload-specific Last-Level Caches.</i> Karthik Swaminathan, Emre Kultursay, Vinay Saripalli, Vijay Narayanan, Mahmut Kandemir (Penn. State U.)
		<i>Low-Power Adaptive RF Systems using Real-time Fuzzy Noise-Distortion Control.</i> Debashis Banerjee (Georgia Institute of Technology); Shreyas Sen (Intel); Aritra Banerjee, Abhijit Chatterjee (Georgia Tech.)
		<i>Designing for Dark Silicon: A Methodological Perspective on Energy Efficient Systems.</i> Jason Allred, Sanghamitra Roy, Koushik Chakraborty (Utah State U.)
		<i>HANDS: Heterogeneous Architectures and Networks-on-Chip Design and Simulation.</i> Davide Zoni, Simone Corbetta, William Fornaciari (Politecnico di Milano)
		<i>XIOSim: Power-Performance Modeling of Mobile x86 Cores.</i> Svilen Kanev, Gu-Yeon Wei, David Brooks (Harvard U.)

# Tuesday, July 31, 2012 (2/3)

TIME	BAY ROOM	REDONDO ROOM
	<i>LogStore: Toward Energy-Proportional Storage Servers.</i> Wei Zheng, Ana Paula Centeno (Rutgers U.); Frederic Chong (UCSB); Ricardo Bianchini (Rutgers U.)	
	<i>A Game Theoretic Resource Allocation for Overall Energy Minimization in Mobile Cloud Computing System.</i> Yang Ge, Yukun Zhang, Qinru Qiu (Syracuse U.); Yung-Hsiang Lu (Purdue U.)	
	<i>A Low-power "Near-threshold" Epileptic Seizure Detection Processor with Multiple Algorithm Programmability.</i> Himanshu Markandeya (Purdue U.); Shriram Raghunathan (Cyberonics Inc.); Pedro Irazoqui, Kaushik Roy (Purdue U.)	
	<i>Understanding the Impact of Laptop Power Saving Options on User Satisfaction Using Physiological Sensors.</i> Matthew Schuchhardt, Ben Scholbrock, Utku Pamuksuz, Gokhan Memik, Peter Dinda (Northwestern U.); Robert P. Dick (U. of Michigan)	
	<i>MultiScale: Memory System DVFS with Multiple Memory Controllers.</i> Qingyuan Deng (Rutgers U.), David Meisner (Facebook), Abhishek Bhattacharjee (Rutgers), Thomas F. Wenisch (UMich), Ricardo Bianchini (Rutgers)	
	<i>Semantics-driven Sensor Configuration for Energy Reduction in Medical Sensor Networks</i> James B. Wendt, Saro Meguerdichian, Hyduke Noshadi, Miodrag Potkonjak (UCLA)	
12:00	<b>Lunch</b>	
13:30 - 15:30	<b>Session 11: Innovations in Low Power Analog</b> Chair: Rajeevan Amirtharajah (UC Davis), Co-Chair: Karthik Kadirvel (Texas Instruments)	<b>Session 12: Software-Driven Techniques for Energy Efficiency in Embedded and Multi-Core Systems</b> Chair: Nikil Dutt (UC Irvine), Co-Chair: Vivek Tiwari (Intel)
13:30	<i>Voltage Droop Reduction for Multiple-Power Domain SoCs with On-Die LDO Using Output Voltage Boost and Adaptive Response Scaling</i> Tetsutaro Hashimoto, Satoshi Tanabe, Kouichi Nakayama, Hisanori Fujisawa (Fujitsu Laboratories Limited)	<i>A Study of the Effectiveness of CPU Consolidation in a Virtualized Multi-Core Server System</i> Inkwon Hwang, Massoud Pedram (USC); Timothy Kam (Intel)

TIME	BAY ROOM	REDONDO ROOM
14:00	★ <i>A 33<math>\mu</math>W 42 GOPS/W 64x64 Pixels Vision Sensor with Dynamic Background Subtraction for Scene Interpretation</i> Nicola Cottini, Massimo Gottardi, Nicola Massari (Fondazione Bruno Kessler); Roberto Passerone (Università di Trento); Zeev Smilansky (Emza Visual Sense Ltd.)	<i>Energy-Efficient Scheduling on Heterogeneous Multi-Core Architectures</i> Jason Cong, Bo Yuan (UCLA)
14:30	<i>Process and Temperature Invariant Bandwidth and Gain, Low-Area, Low-Power and High Swing G<sub>m</sub>-C Filter for Multichannel Neuro-potential Signal Conditioning</i> Anvesha Amaravati, Maryam Shojaei Baghini (IIT-Bombay)	★ <i>MAC: Migration-Aware Compilation for STT-RAM based Hybrid Cache in Embedded Systems</i> Qingan Li, Jianhua Li, Liang Shi, Chun Jason Xue (City U. of Hong Kong); Yanxiang He (Wuhan U.)
15:00	<i>A Charge Pump Based Receiver Circuit for a Voltage Scaled Interconnect</i> Aatmesh Shrivastava, John Lach, Benton Calhoun (U. of Virginia)	<i>Energy-Efficient Signal Processing in Wearable Embedded Systems: An Optimal Feature Selection Approach</i> Hassan Ghasemzadeh, Navid Amini, Majid Sarrafzadeh (UCLA)
	<i>0.35V, 4.1<math>\mu</math>W, 39MHz Crystal Oscillator Circuit in 40nm CMOS</i> Akira Saito (STARC); Yunfei Zheng (U. of Tokyo); Kazunori Watanabe (STARC); Takayasu Sakurai, Makoto Takamiya (U. of Tokyo)	
15:30	<b>Break</b>	

# Tuesday, July 31, 2012 (3/3)

TIME	BAY ROOM	REDONDO ROOM
16:00	<p><b>Design Contest</b> Co-Chairs: Chia-Lin Yang (National Taiwan U), Yiran Chen (U. of Pittsburgh)</p> <p><i>An Ultra Energy Efficient Nonvolatile Processor for Self-powered Sensor Platforms.</i> Yiqun Wang, Yongpan Liu, Shuangchen Li, Daming Zhang, Hongyang Jia, Huazhong Yang, Mei-fang Chiang, Yan-xin Yan and Baiko Sai (Tsinghua University)</p> <p><i>A 14.5 fJ/cycle/k-gate ECG Processor in 45 nm CMOS Using Statistical Error Compensation.</i> Rami Abdallah and Naresh Shanbhag (UIUC)</p> <p><i>First-Generation Hybrid Electrical Energy Storage System.</i> Youngyun Kim, Donghwa Shin, Jaehyun Park, Youngil Kim, Jaemin Kim, Sangyoung Park, Kitae Kim (Seoul National University), Massoud Pedram (University of Southern California) and Naehyuck Chang (SNU)</p> <p><i>An Embedded Flash Memory in a Generic 65nm Logic Process for Zero-Standby-Power System-on-Chip Applications</i> Seung-Hwan Song, Ki Chul Chun and Chris H. Kim (University of Minnesota)</p>	<p><b>Embedded Tutorial:</b> Advanced Power and Thermal Management for Low-Power, High-Performance Smartphones Speaker: Hwisung Jung (Broadcom)</p>

TIME	BAY ROOM	REDONDO ROOM
18:00	<b>Industry Reception</b>	
19:00	<b>Social Event - Banquet</b>	

# Wednesday, August 1, 2012

TIME	BAY ROOM	REDONDO ROOM
7:30	<b>Breakfast</b>	
8:30	<b>Keynote:</b> Ultra-Low Power Challenges for the Next Generation ASIC Speaker: Uming Ko, MediaTek USA Chair: Ajith Amerasekera (Texas Instruments)	
9:30	<b>Break</b>	
10:00 - 12:00	<b>Session 13: Processor Design and Implementation</b> Chair: Lawrence Clark (Arizona State U. and SuVolta, Inc.), Co-Chair: Sujat Jamil (Marvell)	<b>Session 14: Memory Management and Scheduling</b> Chair: Naehyuck Chang (Seoul National Univ.), Co-Chair: Guangyu Sun (Peking Univ.)
10:00	<i>The Core-C6 (CC6) Sleep State of the AMD Bobcat x86 Microprocessor</i> Aaron Rogers, David Kaplan, Eric Quinnell, Bill Kwan (AMD Austin)	<i>Reducing L1 Caches Power By Exploiting Software Semantics</i> Zhen Fang (NVIDIA); Li Zhao, Xiaowei Jiang, Shih-lien Lu, Ravi Iyer, Tong Li (Intel Corp.); Seung Eun Lee (Seoul National University of Science and Technology)
10:30	<i>Evaluation of Voltage Stacking for Near-Threshold Multicore Computing</i> Sae Kyu Lee, David Brooks, Gu-Yeon Wei (Harvard University)	<i>DRAM Power-Aware Rank Scheduling</i> Sukki Kim (LG Electronics), Soontae Kim, Yebin Lee (Korea Advanced Institute Science and Technology)
11:00	<i>CHARM: A Composable Heterogeneous Accelerator-Rich Microprocessor</i> Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Beayna Grigorian, Glenn Reinman (UCLA)	<i>Energy-Efficient GPU Design with Reconfigurable In-Package Graphics Memory</i> Jishen Zhao (The Pennsylvania State University); Guangyu Sun (Peking University); Gabriel H. Loh (AMD); Yuan Xie (PSU & AMD)

TIME	BAY ROOM	REDONDO ROOM
11:30	<i>Something Old and Something New: P-States Can Borrow Microarchitecture Techniques Too</i> Yasuko Eckert (AMD & U. of Wisconsin-Madison), Srilatha Manne, Michael J. Schulte (Advanced Micro Devices); David A. Wood (University of Wisconsin-Madison & AMD)	<i>Fan-Speed-Aware Scheduling of Data Intensive Jobs</i> Christine S. Chan, Yanqin Jin, Yen-Kuan Wu (University of California, San Diego); Kenny Gross, Kalyan Vaidyanathan (Oracle Physical Sciences Research Center); Tajana Šimunić Rosing (UCSD)
		<i>Procedure Hopping: a Low Overhead Solution to Mitigate Variability in Shared-L1 Processor Clusters</i> Abbas Rahimi (University of California, San Diego); Luca Benini (Università di Bologna); Rajesh Gupta (UCSD)
12:00	<b>Closing</b>	