Challenges in Low-Power Analog Circuit Design for sub-28nm CMOS Technologies

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Outline

• Scaling Effects
• Design Methodology
• Challenges in sub-28nm CMOS
• Analog Design for sub-28nm CMOS
• Design Examples
• Conclusions
Scaling Effects

- Transistor cross section:

\[ V_s = \frac{C_{ox} \cdot V_g + C_d \cdot V_d}{C_{ox} \left(1 + \frac{C_d}{C_{ox}}\right) + C_{dep}} \]

\[ \Rightarrow V_s \propto V_d \]

\[ V_b = \frac{C_{oxe} \cdot V_g + C_d \cdot V_d}{C_{oxe} \left(1 + \frac{C_d}{C_{oxe}}\right) + C_{dep}} \]

\[ \Rightarrow I_{leakage} \text{ more in deep substrate} \]

Where: \[ C_{oxe} = \frac{C_{ox} \cdot C_{dep1}}{C_{ox} + C_{dep1}} \]

- Known as drain induced barrier lowering (DIBL)
- As L scales: 1) Cox↑ 2) W_{dep}↓(body doping)
Scaling Effects

• Leakage current scaling (W=1um)

\[ I_D = I_{S0} W e^{\frac{q}{K T} (V_{GS} + B V_{DS})} \]
Scaling Effects

- **Intrinsic Transistor Gain:** \( A_v = g_m \cdot r_o \)
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Design Methodology

- Important Figure-of-merit in analog design is the $G_m/I_{DS}$ ratio
Design Methodology

• Other important metrics in analog design include:
  • **Noise**: limits the minimum detectable signal (MDS) that the analog circuit can process
  • **Linearity**: limits the maximum possible signal that the analog circuit can process

![Diagram](https://via.placeholder.com/150)

\[ IIP_3 (dBm) = P_{BL} (dBm) + \frac{P_{BL} (dBm) - P_{IM3} (dBm)}{2} \]

• Noise+Linearity → define the “dynamic range” (DR) of the signal that the circuit can handle

\[ DR = \frac{2}{3} (IIP_3 - MDS) \]
Design Methodology

• Other important metrics in analog design include:
  • Gain \(g_m\), Bandwidth \(F_t\), power consumption

• Define a “figure-of-merit” (FOM) to take into account dynamic range and bandwidth
  • This FOM describes maximum performance without regard to power consumption

\[
FOM = 10 \log(f_T) + \frac{2}{3} \left[ IIP3 - 10 \log \left( \int v_n^2 df \right) \right]
\]

Bandwidth

Dynamic range
Design Methodology

• FOM plot over current consumption:

\[
FOM = 10 \log(f_T) + \frac{2}{3} \left( IIP3 - 10 \log \left( \int v_n^2 df \right) \right)
\]
Design Methodology

• Define another “figure-of-merit” (FOM2) to take into account current consumption as well
  • FOM2 takes into account the current efficiency in obtaining a certain performance level

\[
FOM2 = 10 \log\left(\frac{g_m}{I_{ds}}\right) + 10 \log(f_T) + \frac{2}{3} \left(\text{IIP}_3 - 10 \log\left(\int n^2 df\right)\right)
\]
Design Methodology

- FOM2 plot over current consumption

\[
FOM 2 = 10 \log \left( \frac{g_m}{I_{ds}} \right) + 10 \log (f_T) + \frac{2}{3} \left( IIP3 - 10 \log \left( \int v_n^2 df \right) \right)
\]
Design Methodology

• Overall design methodology:
  1. Generate parametric curves based on FOM or FOM2 (Ids and W are parameters)
  2. ChooseIds and W that meet desired specifications
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Challenges in sub-28nm CMOS

• Stress effects (isolation proximity):
  • Stress = Force / Area
  • Stress scenarios:
    1. Force = q * E
    2. Stress is also induced by interface boundaries between material with different dopant densities (adjacent NFETs or NFET/PFET boundary)

• Effect of stress → carrier mobility shifts (current!)
• Mitigate by use of dummies & equally spaced devices
Challenges in sub-28nm CMOS

- Diffusion proximity (well proximity)
  - Dopant atoms scattered from adjacent photoresist

Scattering → variability in doping profile

**VT variation in order to 10’s mV**

- Mitigate by use of dummies

Source: Freescale Semiconductor (0.13um 3.3V NFET)
Challenges in sub-28nm CMOS

- Device gate leakage:
  - Gate leakage caused by quantum tunneling effect

\[ i_{GS} \approx C_{ox} \cdot W \cdot L \cdot f_{gate} \]

Introduction of HK/MG
Challenges in sub-28nm CMOS

• Gate leakage introduce low-frequency pole:

\[ R_g = \frac{1}{g_{\text{tunnel}}} \]

\[ f_{\text{gate}} = \frac{g_{\text{tunnel}}}{2\pi C_{\text{in}}} \]

• This creates a low-frequency bound on sample-and-hold (S/H) circuits as well as low-frequency RC filters (such as PLL loop filters)
Challenges in sub-28nm CMOS

• Gate leakage causes mismatch in current mirrors:

Classical mismatch:

\[
\left( \frac{\Delta I}{I} \right)^2 = \left( \frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I} \right)^2
\]

Mismatch with gate tunneling:

\[
\left( \frac{\Delta I}{I} \right)^2 = \left( \frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I} \right)^2 + \left( \frac{X_{IGS} \cdot i_G}{\sqrt{WL} \cdot I} \right)^2
\]
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Sub-28nm CMOS Circuit Design

- Stack devices
  - Ensure no stressed oxides during off mode
  - Used in I/O drivers
Sub-28nm CMOS Circuit Design

• Digitally assisted analog circuit design
  • Use trimming/calibration loops to sense imperfections in analog circuits → mismatches, center frequency, etc.

• Data converters (DAC/ADC):
  • Use a higher resolution, lower frequency ADC/DAC to sense imperfections
  • Input voltage (or digital word) is a saw-tooth waveform during calibration

• VCO:
  • Trim center frequency
  • Trim LC tank amplitude
Sub-28nm CMOS Circuit Design

- Design techniques:
  - Digital temperature sensor \(\rightarrow\) use to adjust analog settings

![Circuit Diagram]

Multiple programmable PFETs

Calibration Logic

Digital output
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Design Examples

• 9-bit SAR ADC in 28nm CMOS

Performance Summary:

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td># bits</td>
<td>9</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>0.9</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>900MHz</td>
</tr>
<tr>
<td>Area</td>
<td>200um x 100um</td>
</tr>
<tr>
<td>Power</td>
<td>382uW</td>
</tr>
<tr>
<td>ENOB</td>
<td>8.51</td>
</tr>
</tbody>
</table>
Design Examples

• 10-bit current steering DAC in 28nm CMOS

Performance Summary:

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td># bits</td>
<td>10</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>0.9</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>200MHz</td>
</tr>
<tr>
<td>Area</td>
<td>200um x 100um</td>
</tr>
<tr>
<td>Power</td>
<td>330uA</td>
</tr>
<tr>
<td>ENOB</td>
<td>8.8 bits</td>
</tr>
</tbody>
</table>
Design Examples

• VCO in 28nm CMOS:

PFET current mirror with embedded PSR

Current amplitude loop to suppress LO harmonics in LC tank.

Performance Summary:

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{osc,center}$</td>
<td>3GHz</td>
</tr>
<tr>
<td>Tuning range</td>
<td>800MHz</td>
</tr>
<tr>
<td>PN @ 1MHz</td>
<td>-134.3dBc/Hz</td>
</tr>
<tr>
<td>Power</td>
<td>9mA</td>
</tr>
</tbody>
</table>
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Conclusions

• Scaling Effects Reviewed
• Design Methodology
  • Based on gm/ID design methodology
  • Extended to include DR & BW
Conclusions

• Challenges in sub-28nm CMOS analog design

<table>
<thead>
<tr>
<th>DSM effect</th>
<th>Analog Circuit Implication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stress effects (isolation proximity)</td>
<td>Mobility variation (BW, current mismatch, gain)</td>
</tr>
<tr>
<td>Diffusion proximity</td>
<td>VT variation (mismatch)</td>
</tr>
<tr>
<td>Gate leakage</td>
<td>Noise, mismatch, low-frequency limit</td>
</tr>
</tbody>
</table>

• Analog circuit design techniques

<table>
<thead>
<tr>
<th>Design Technique</th>
<th>Reason / Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>FET stacking</td>
<td>High voltage swing</td>
</tr>
<tr>
<td>Digital assist / temp sensor</td>
<td>Trimming analog</td>
</tr>
</tbody>
</table>

• Design examples: DAC, ADC, VCO