Process and Design Solutions for Exploiting FD-SOI Technology Towards Energy Efficient SOCs

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STMicroelectronics
28nm Planar UTBB FD-SOI Transistor

Substrate

High-K Metal Gate

Thin Body (7nm)

Thin BOX (25nm)

Ultra Thin Body & BOX Fully Depleted SOI transistor
28nm Planar UTBB FD-SOI Advantages

- Shorter channel length
  - 24nm technology!
- Better electrostatics
  - Faster operation
  - Low voltage
  - Reduced variability
- Total dielectric isolation
  - Latch up immunity
- Lower leakage current
  - Less sensitive to temperature
Body Biasing (BB)

A very reasonable effort for extremely worthwhile benefits

- An **extremely powerful** and flexible concept in FD-SOI to:
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts

- Comparatively **easy to implement** – if you’ve ever done DVFS you’ll have no difficulty with Body Biasing
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control
Extended Body Bias Range in UTBB FD-SOI

BULK

-300mV $\rightarrow$ FBB $\rightarrow$ RBB $\rightarrow$ noBB $\rightarrow$ +300mV

UTBB FD-SOI

NMOS

-3V $\rightarrow$ RBB $\rightarrow$ noBB $\rightarrow$ FBB $\rightarrow$ +3V

PMOS
UTBB FD-SOI: Extended Body Voltage Range

- **Conventional Well (CW) - RBB**

   - NMOS
   - PMOS
   - Gndsn
   - Vddsp
   - f-Well
   - n-Well
   - Gndsp

- **Flip Well (FW) - FBB**

   - NMOS
   - PMOS
   - Gndsp
   - Gndsn
   - f-Well
   - n-Well

Efficient knob for speed/leakage optimization
Body Bias Efficiency - Silicon Evidence
FBB usage per market segment

Infrastructure - Networking
Servers and Storage

Supply: 0.7 – 0.9V
high number multicore
DVFS & FBB tuning for best
MIPS/W ratio.
Adapt perf&power to workload

28 FD-SOI:
Up to -50% total power reduction
versus 28G(mobile) @ 0.6V
FBB for ultimate power efficiency
tuning

Consumer

Supply: 0.6 –1.1V
Wide DVFS
FBB linked to CPU workload
& thermal conditions

28 FD-SOI:
Up to -50% power reduction
FBB provides +18%
max. performance boost
versus 28G(mobile)

Ultra-Low-Energy

Ultra Low
Voltage 0.3V-
0.4V
Reverse Body
Biasing

Internet of Things

Supply: 0.6V-0.9V
FBB: 0 - 1.5V
FBB to solve the
power/performance
paradigm

µAP

Ultra power efficiency

8
Improved Memory Minimum Voltage

Vddmin on 0.120µm² bitcell

Vmin gain thanks to better mismatch on FD-SOI devices (undoped channel)
FD-SOI Unique "Single Well" Architecture

**SRAM regular wells**

**SRAM flip-well architecture**

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**Single Well SRAM**

Optimized stability helping behavior at low voltage

➔ Power efficiency

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**ST patented bitcell architecture**

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![Graph showing probability of Vddmin for regular wells and single well SRAM](image1)

**Vddmin ±70mV**

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![Graph showing Vddmin (V) vs. Probability (%) for regular wells and single well SRAM](image2)
Si Evidence: LDPC on UTBB FD-SOI

LDPC 6T-SRAM (FBB 1V) functional down to 0.41V

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Ultra-Wide Body-Bias Range LDPC Decoder in 28nm UTBB FD-SOI
State of the Art UWVR DSP in FDSOI:

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27.1: A 460MHz@397mV – 2.6GHz@1.3V 32bit VLIW DSP
Cortex A9: FD-SOI allowing Ultra-Wide DVFS

- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
  - >5x when compared to 28LP technology
  - >35% when compared to 28G technologies

- DVFS energy efficiency optimization is further extended thanks to body bias
  - Allowing to balance and optimize the static and dynamic power consumption components
Cortex A9 Power vs. Performances

A9 Single Dhrystone power consumption
28nm FD-SOI Best in class efficiency

- @ low Vdd
  - +43% vs 28LP
  - +83% vs 28G

- @ high Vdd
  - +50% vs 28LP
  - +25% vs 28G

Graph showing energy efficiency vs speed (relative DMIPS) at low and high Vdd conditions. FD-SOI 28nm outperforms bulk 28nm G and LP at both Vdd conditions, with significant improvements over 28LP and 28G.
Faster, Cooler, Simpler technology

- FD-SOI transistors up to 30% faster than bulk
- Outstanding power efficiency at every level
- Extensive use of existing fab infrastructure

Enhanced design options

- Back-biasing as a flexible and powerful optimization
- Very large operating range for the same design
- Ultra-wide range DVFS

Mature process & ecosystem

- Ecosystem ready at all stage: wafer supply, design and manufacturing
- Extended IP offer
- Strategic collaboration between Samsung and ST

FD-SEI gives your SOC competitive advantages