A New Silicon Age 4.0: Generating Semiconductor-Intelligence Paradigm with a Virtual Moore's Law Economics and Heterogeneous Technologies

Nicky Lu, Ph.D., IEEE Fellow, NAE (USA) Member

CEO, Chair & Founder, Etron Technology, Inc.

Chair, TSIA (Taiwan Semiconductor Industry Association, 2013-17)

Chair, GSA (Global Semiconductor Alliance, 2009-11)

Chair, WSC (World Semiconductor Council, 2014-15)

Outstanding Alumnus, National Taiwan University & National Chiao-Tung University

July 24, 2017

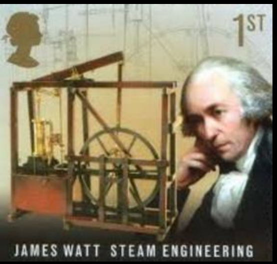
On IC-Industry Future：A Personal View

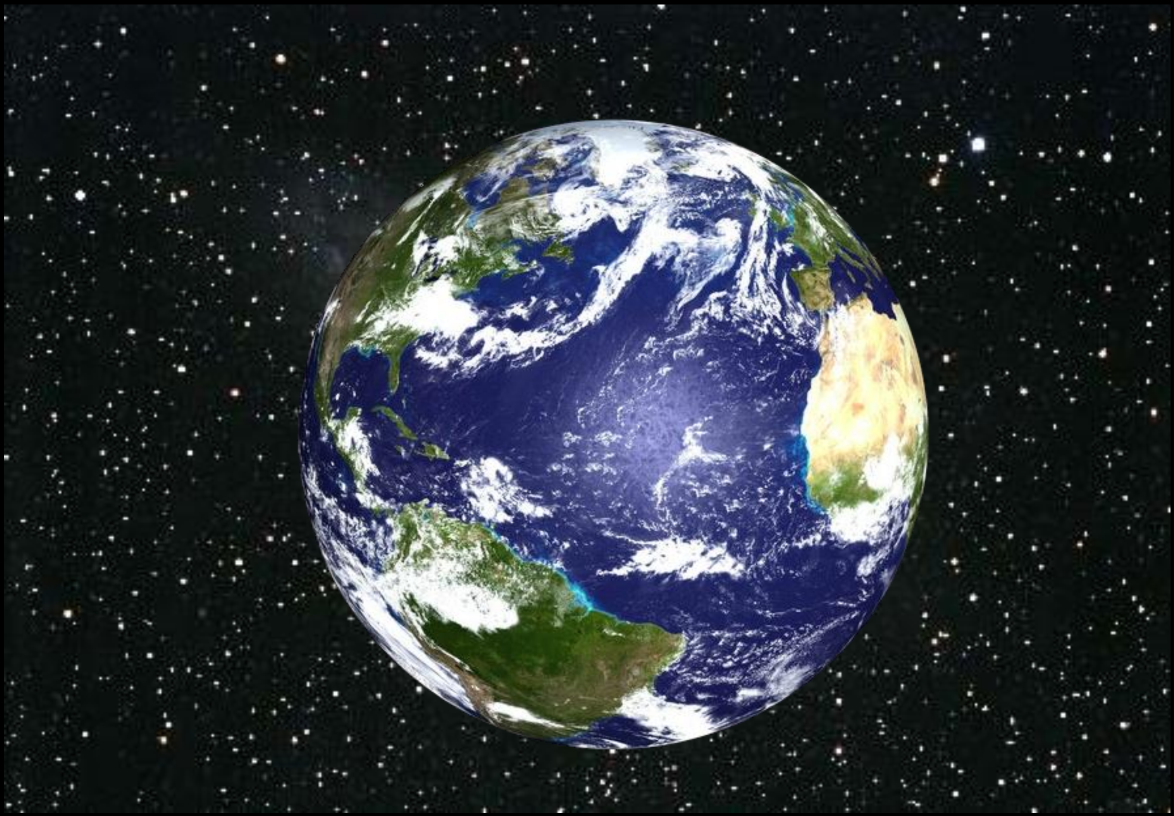
This talk simply presents my personal analytical and semi-quantitative assessment on the future fate and economic value of the IC/Microelectronics Industry, as it trends towards atomic-scale nano-system through innovative value-creation scaling, both down and up, by adopting Heterogeneous Integration of Silicon + Non-Silicon Composition.

Acknowledgments

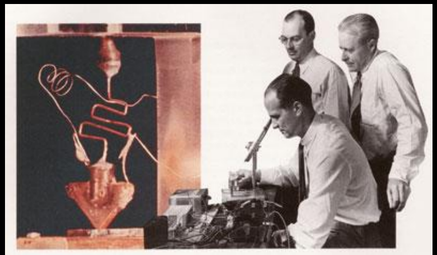
Mickey Ken	Douglas Yu	Jack Sun	Bill Bottoms
Sam Pan	CY Lu	Richard Crisp	Bill Chen

Earth & Human-Civilization Enriched from the Industrial Revolution to the Science-and-Technology Revolution





Silicon Age Started in the Mid-20th Century



An Emerging Transformative Revolution in 21st Century

- A Revolution Driven by Diverse&Boundless Smart Applications Enabled by Science& Technology Advancement
  - Many Ways of Artificial and Machine Intelligences
  - Power Stems from Integrated Circuits, Algorithm, System & Software
  - Computerized DNA/Cell/Microbiome Personalized Medicine for Longer Life

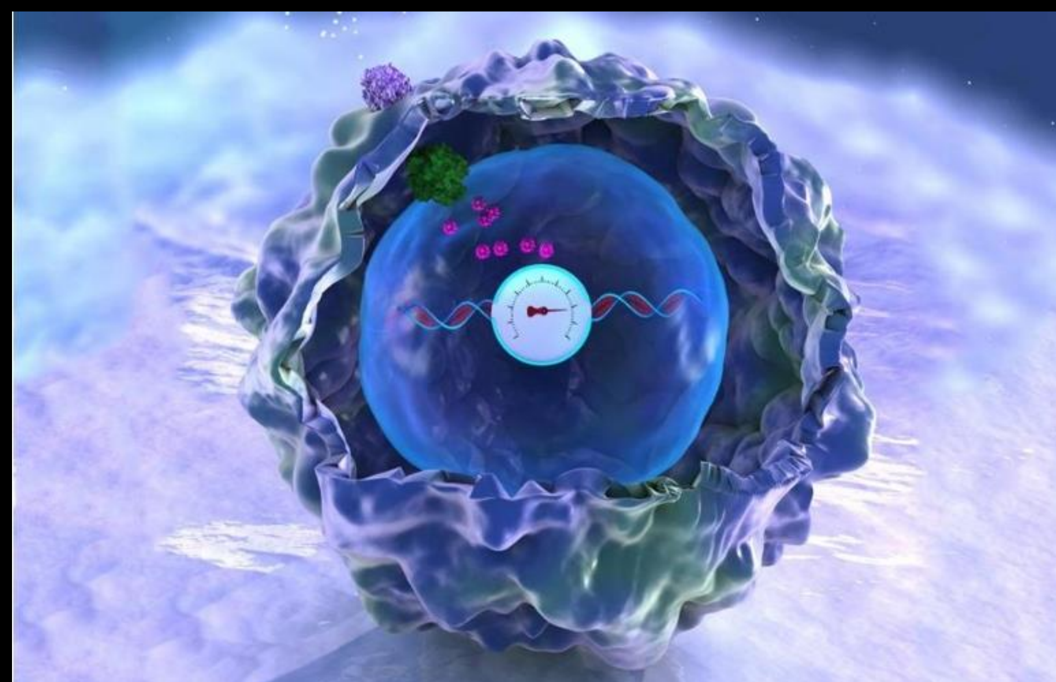
Cloud Computing, Big Data, Machine/Deep Learning, and the Revival of AI

Technology's Diverse and Boundless Applications (Example I)

Innovative Genetic Engineering to Improve Human Life:
Microbiome therapies, Synthetic Biology, Genome Editing
Technology's Diverse and Boundless Applications (Example II)

Source: Scientific American, June, 2016

Recording the secret lives of cells (Cancer, Parkinson's Disease…normal)



Source: Hartnett, the Boston Globe, September, 2016

After Timothy Lu, Science, Nature, etc.

20th Century：Human Did Fly by Air Plane;

21st century：By Rocket Plane ?

Technology's Diverse and Boundless Applications (Example III)

LAUNCH. LAND. REPEAT.

JANUARY 22, 2016

West Texas Launch Site

BLUE ORIGIN

Human Life Being Enriched by Many Applications Created by Nanometer Silicon-Intelligence Paradigms

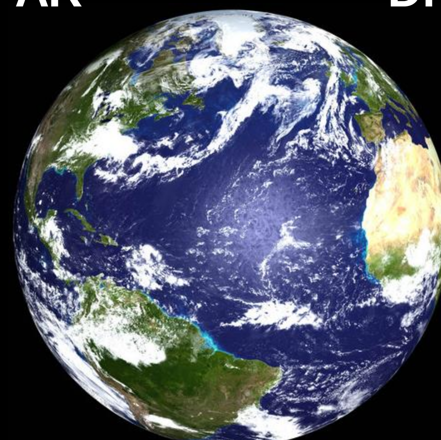

Real-time Video Streaming


VR / AR


Drone


Robot Safety System


3D Scan and Printing




Wearable

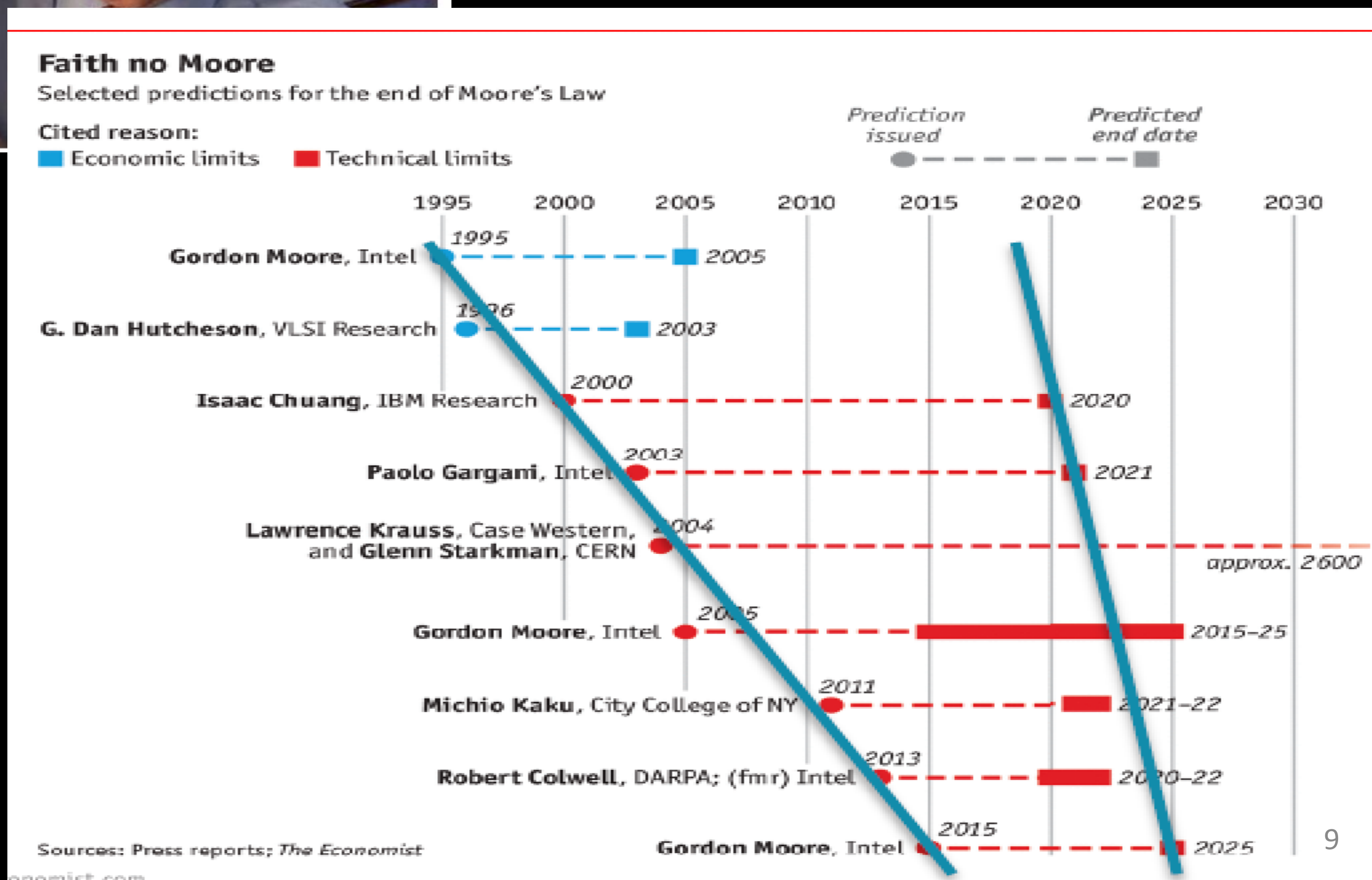

Smart Car


Smart Home


Smart City


Smart Health Care

But, Will the Driving Engine of Silicon Growth, Moore's Law, Die as We Approach 2025?



The Economist explains

The end of Moore’s law

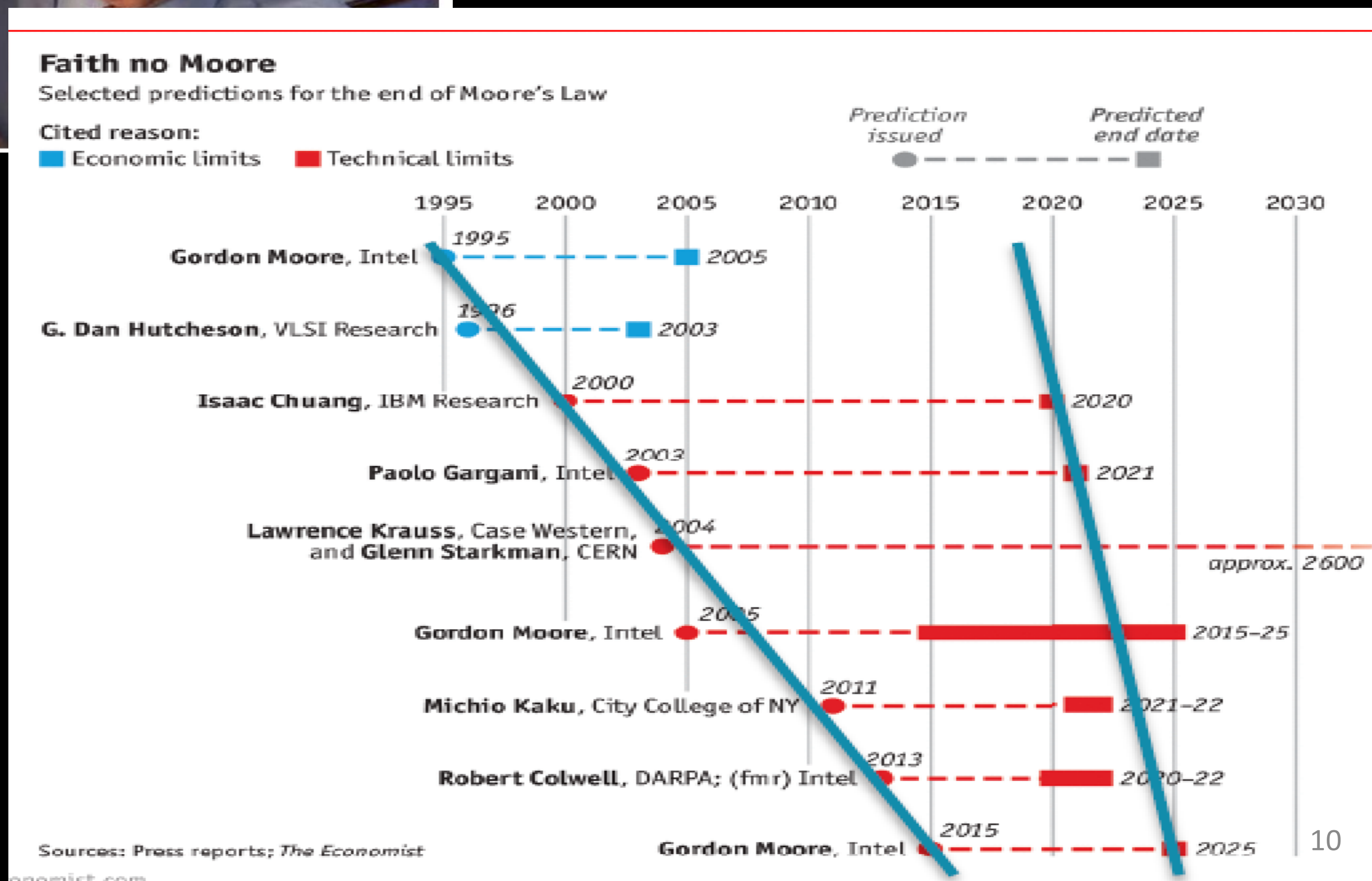
The Economist

Apr 19th 2015, 10:38 BY L.S.

Timekeeper

Tweet

What is Our Semiconductor Industry’s View?



No Exponential is Forever: But "Forever" Can Be Delayed! Gordon Moore, ISSCC 2003

Moore's Law – It's All About Economics

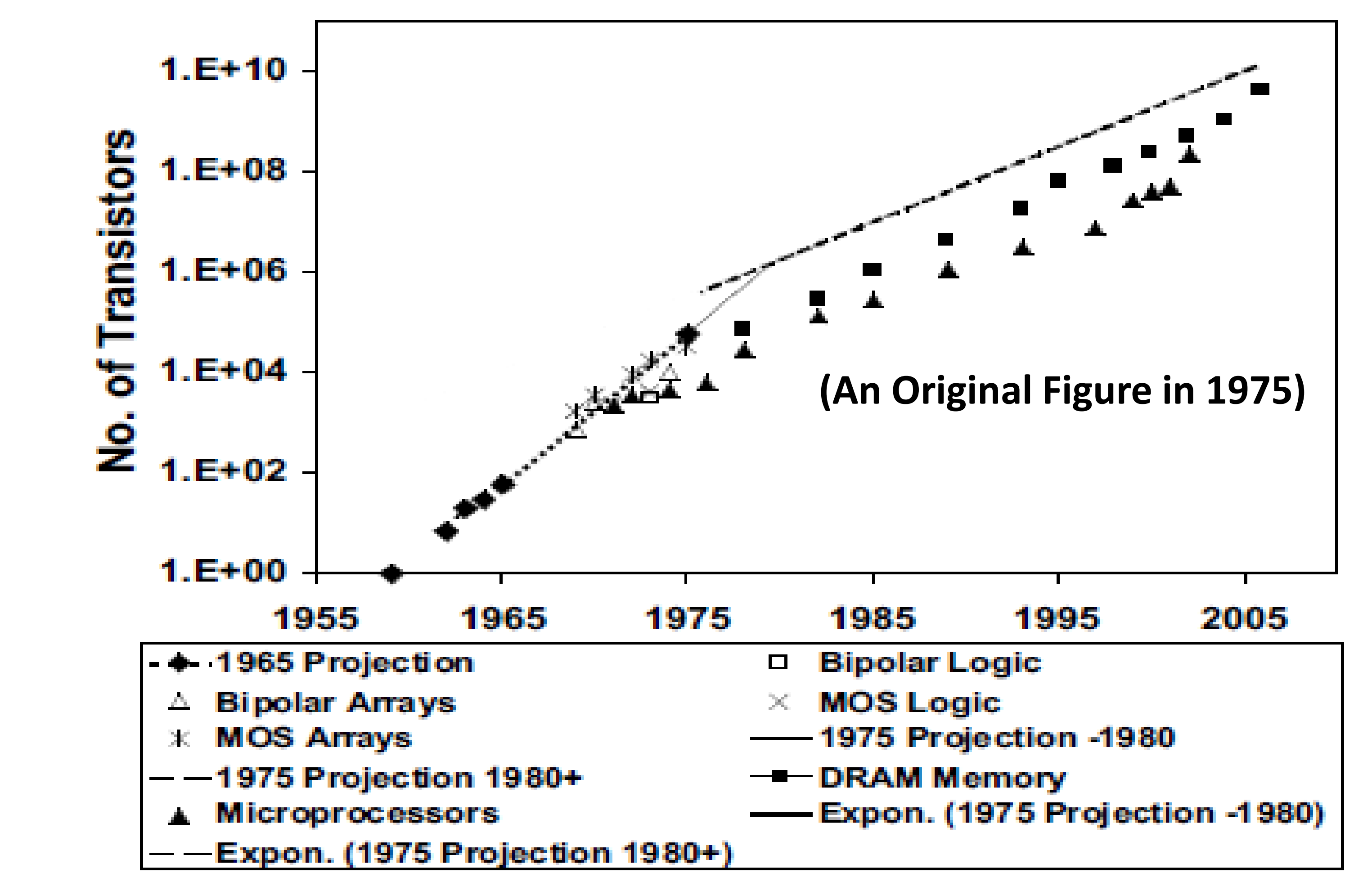
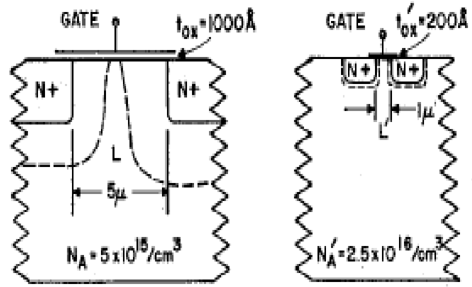


Figure 1.1.8: 1975 transistor projection with data.

Dennard's Line Scaling theory

Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

ROBERT H. DENNARD, MEMBER, IEEE, FRITZ H. GAENSSLEN, HWA-NIEN YU, MEMBER, IEEE, V. LEO RIDEOUT, MEMBER, IEEE, ERNEST BASSOUS, AND ANDRE R. LEBLANC, MEMBER, IEEE



(a) (b)

Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

1974

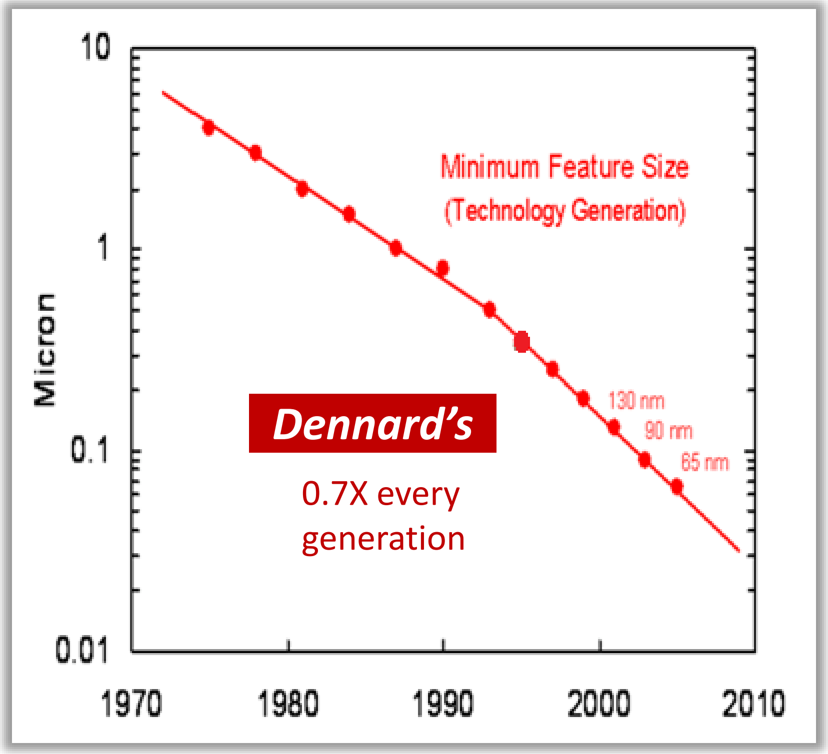
BOLS
logarithmic slope of sub-
haracteristic.
alized step function pro-
nnel implant.
n difference between gate
ate.
nstants for silicon and
ide.
t.
constant.
ng constant.
annel length.
face mobility.
ier concentration.
eptor concentration.
g in silicon at the onset of
ersion for zero substrate

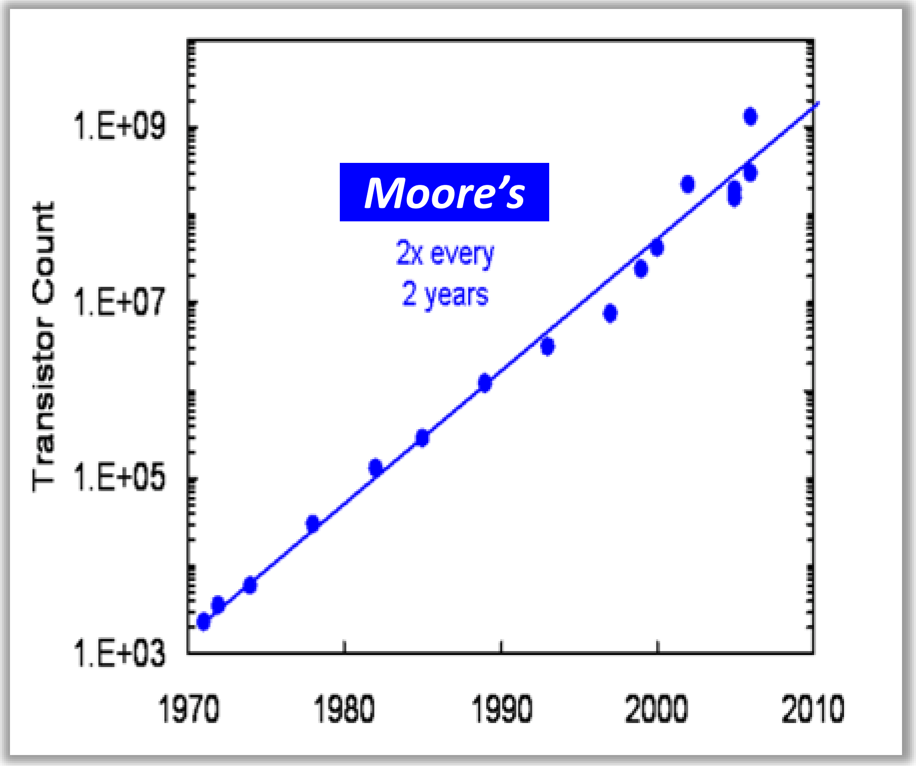
Table 1
Scaling Results for Circuit Performance

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Credit : R. Dennard, IBM 1974

Dennard's Line Scaling ($1/\alpha^2$=2X if α =0.7X) Explained Moore's Law : 2X #Transistors per Every Generation



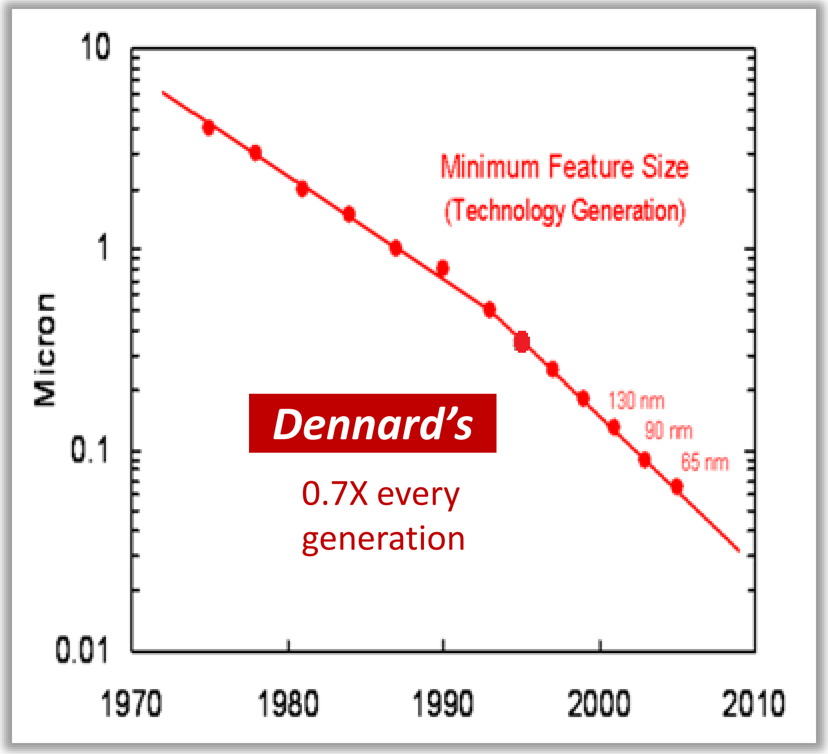


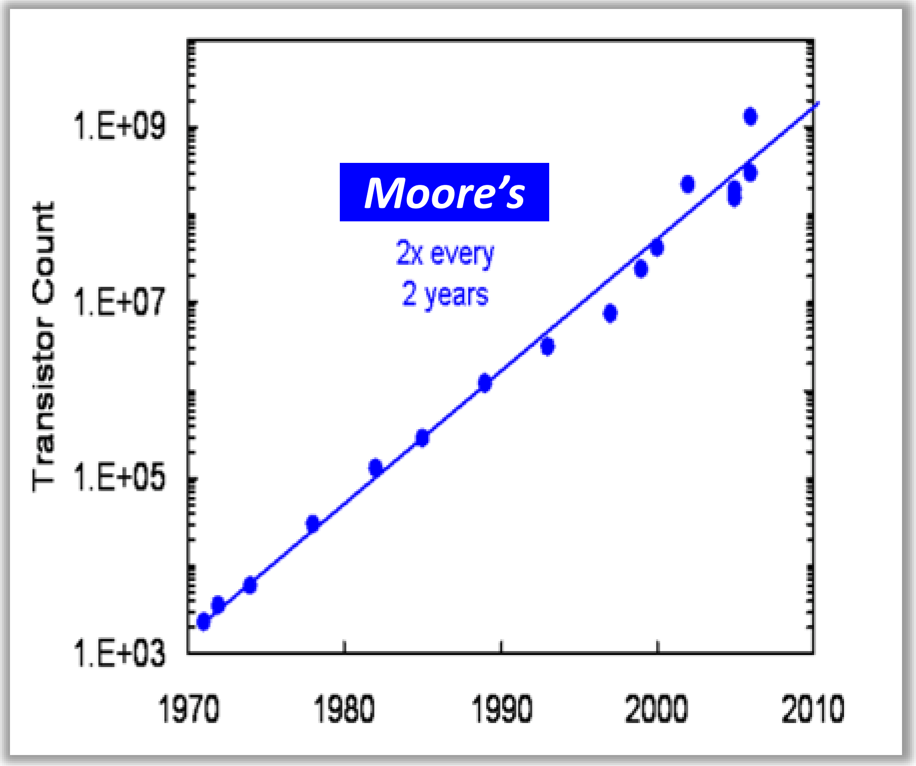
Credit : R. Dennard, IBM 1974, G. Moore, Intel 1975

Dennard's Line Scaling ($1/\alpha^2$=2X if α =0.7X) Explained

Moore's Law : 2X #Transistors per Every Generation

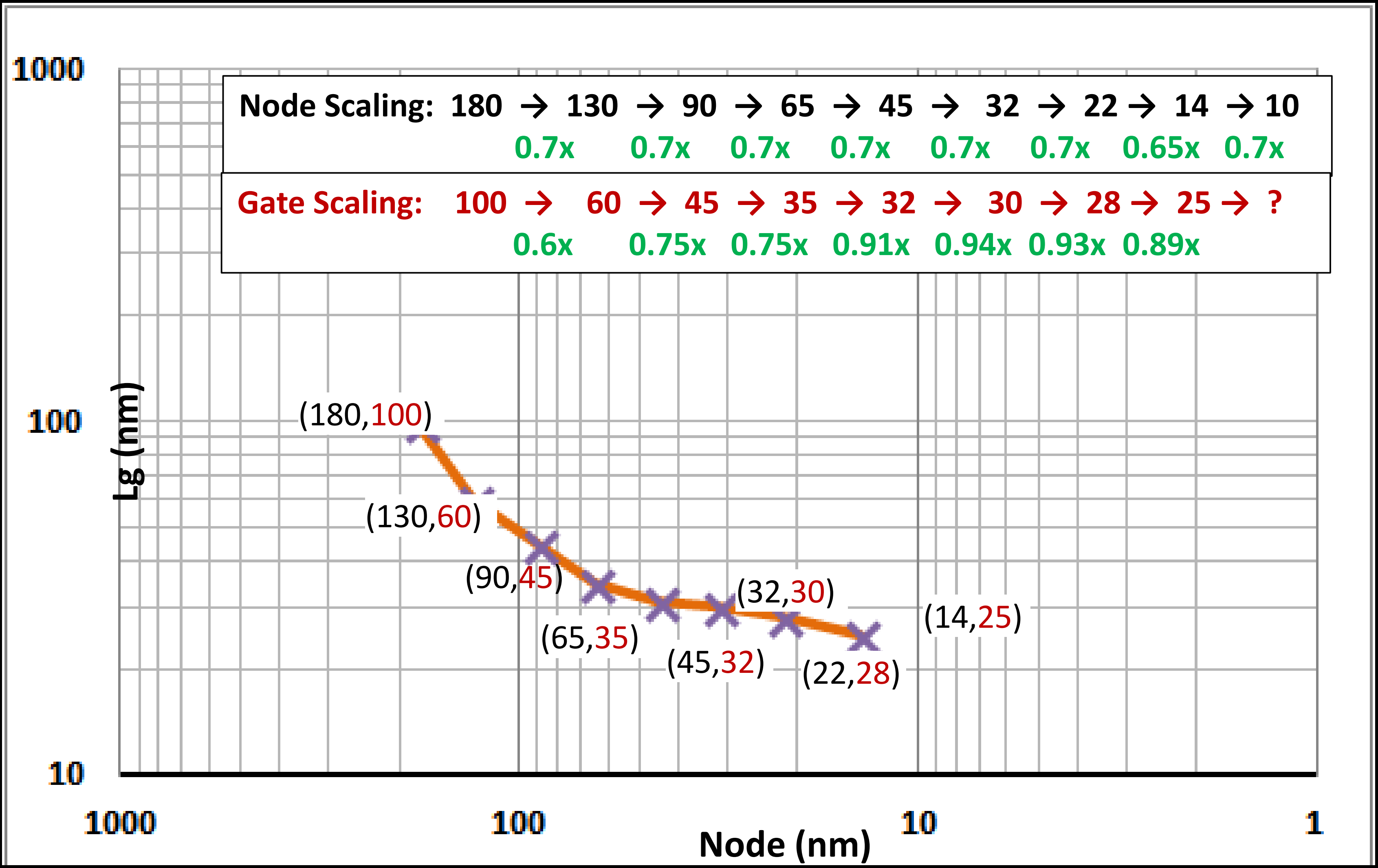
Silicon Age 1.0 (Si1.0) : 0.7X Scaling 20 Nodes Well Followed Line-Scaling + ME (Moore's Law Economy) to Go from 30μm to 28nm





Source: R. Dennard, IBM 1974; G. Moore, Intel 1975

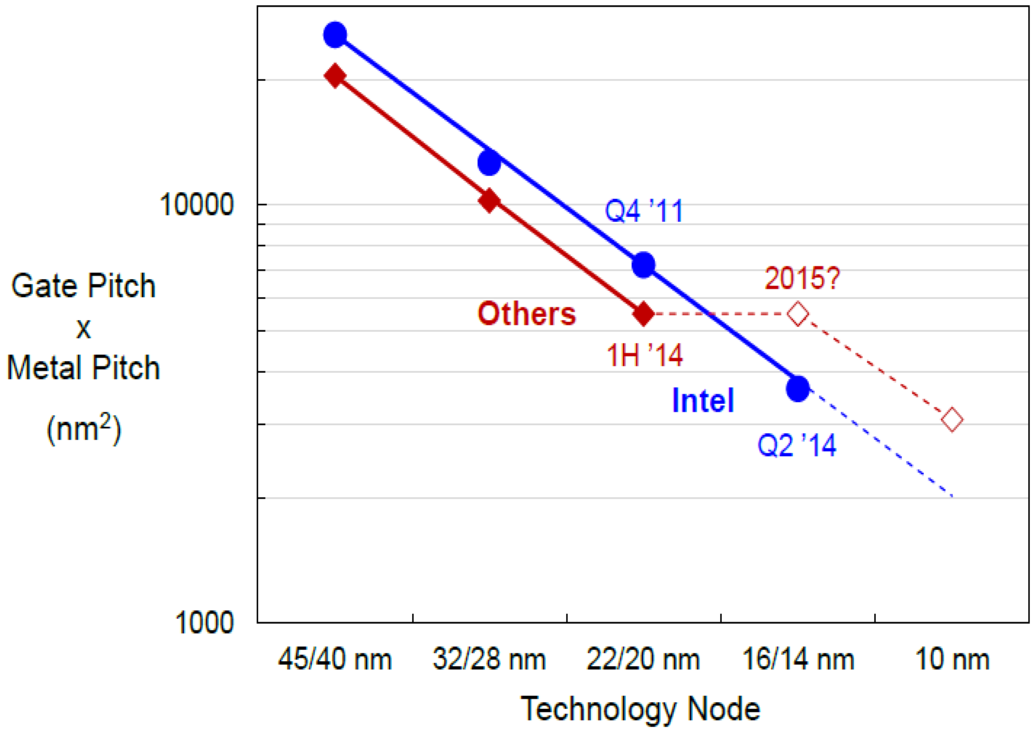
Node Scaling Still Follows 0.7X, but Gate Length Has Departed from It : Reversed Line Scaling ?



Source: Intel Publications; Wikipedia 2016 and Estimated

Logic Competition: Area Scaling (I)

Logic Area Scaling



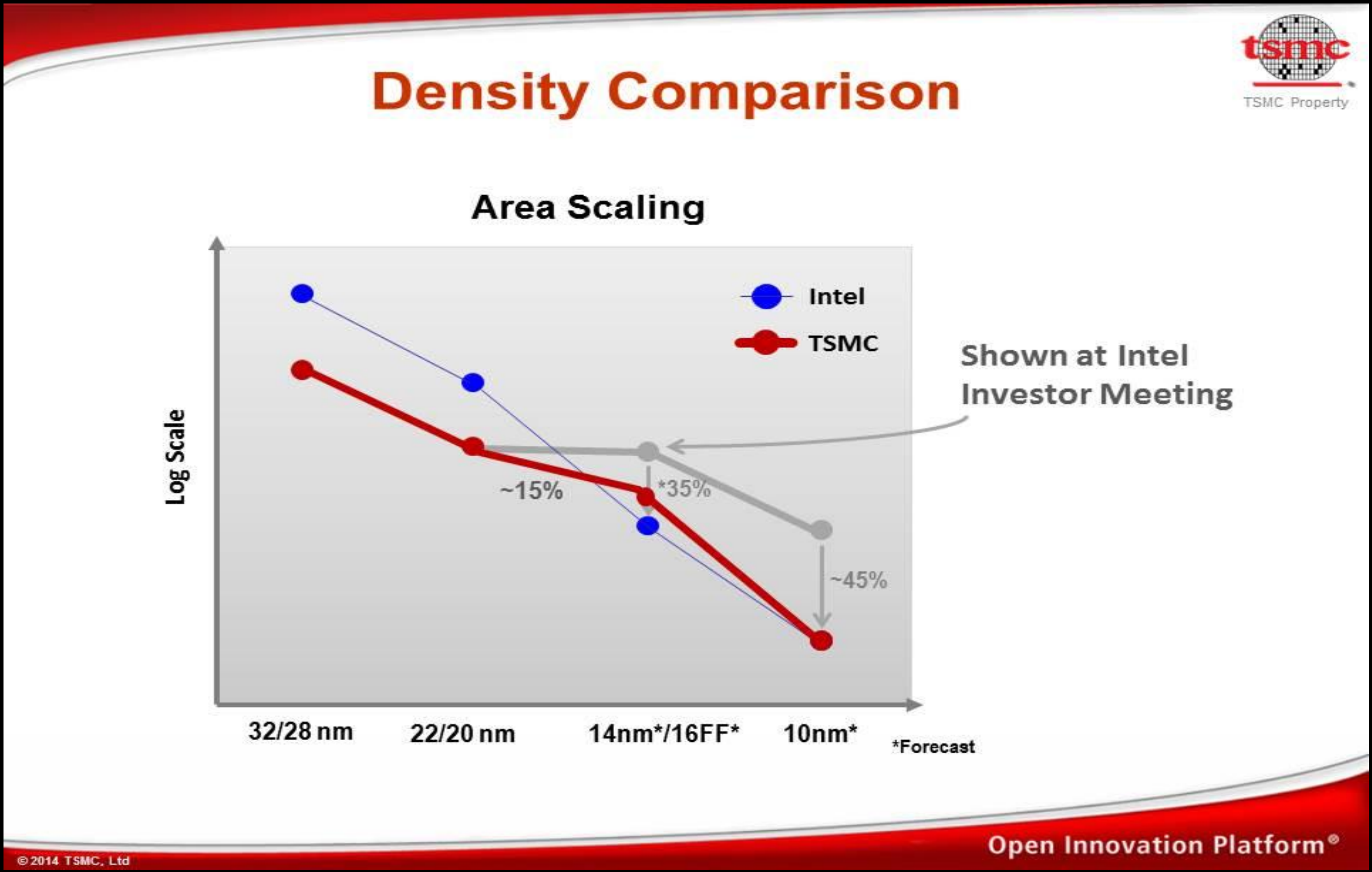
Intel 14 nm is both denser and earlier than what others call "16nm" or "14nm"

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p.129
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14

31 IDF14

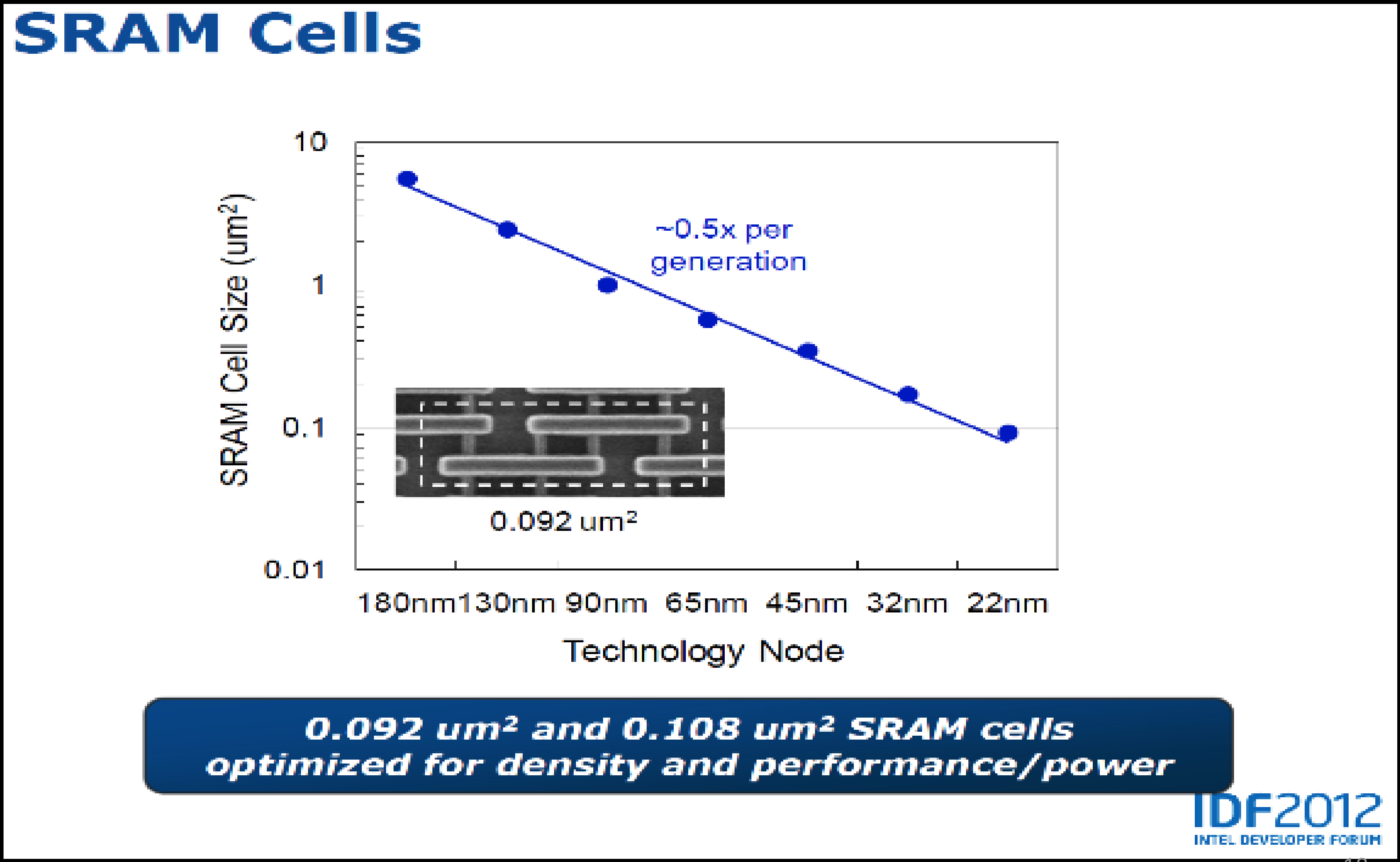
Source: Intel IDF 2014

Logic Competition: Area Scaling (II)



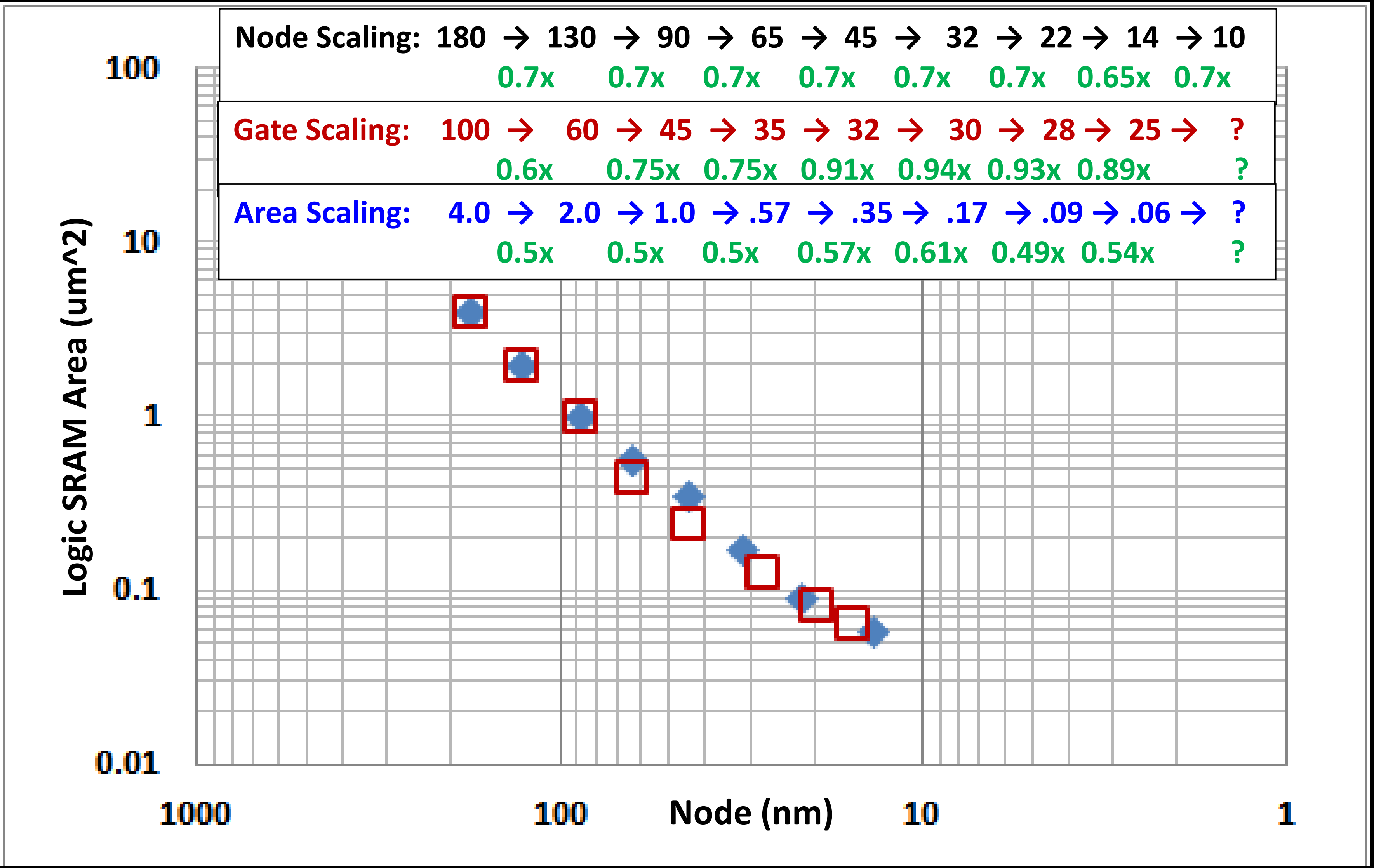
Sources: SemiWiki Jan.21 2014 and TSMC

SRAM-Cell Area Scaling (I)



Source: Intel IDF 2012

Logic/SRAM Area-Scaling after Gate Line-Scaling



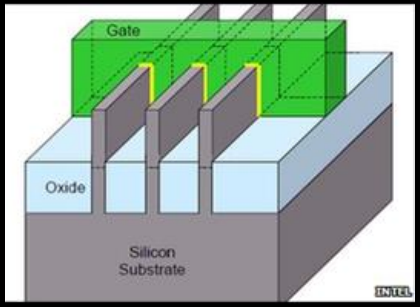
Sources: Intel IDF 2012; IEDMs; VLSI Conferences and Estimated

A New Area-Scaling Method Creating An EME (Effective Moore's Law Economy)：Silicon 2.0 (Si2.0) - 22/20 to ~7nm

2D
Line
Scaling
(Planar)

(Si1.0)

3D Areal Density or
Area Scaling
3D FinFET+(>0.7X
Line-Scaling) Continues
Moore's 2X Law



TSMC Leading Foundry 3D Areal Density Scaling:
10 nm Production 2016;
Outlook: 7 nm production in 2018, 5 nm 2020

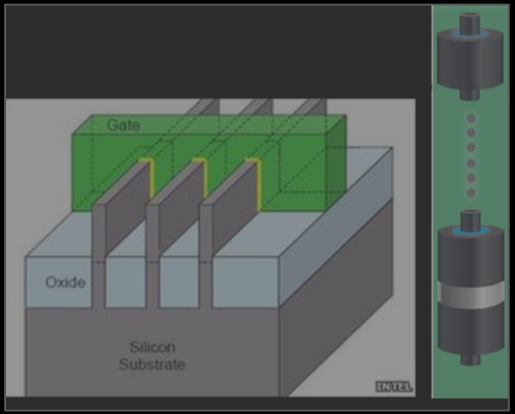
Fig. 4. A Sketch of Silicon Age 2.0 due to an Area-Scaling Methodology [8,9,10] Which Creating an Effective Moore's Law Economy(EME), A-SSCC2016

Another Volume-Scaling Method Is Happening in the Effective Moore’s Law Economy (EME)

2D
Line
Scaling
(Planar)

(Si1.0)

3D Areal Density or
Area Scaling
3D FinFET+(>0.7X
Line-Scaling) Continues
Moore’s 2X Law



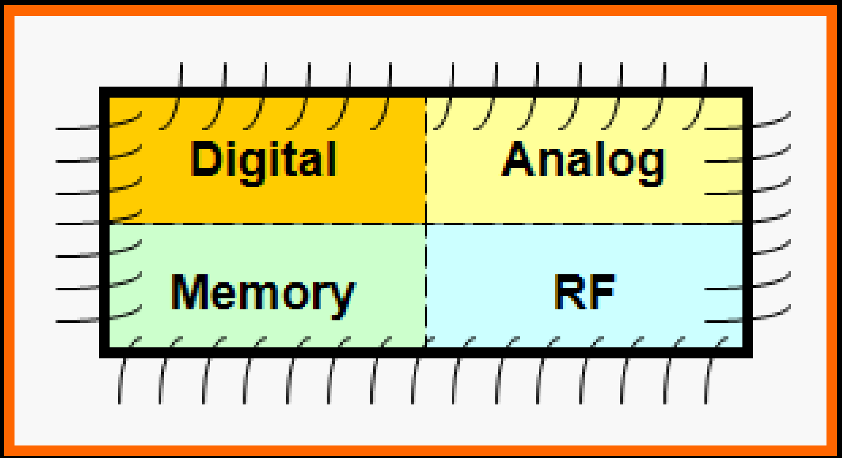
TSMC Leading Foundry 3D Areal Density Scaling:
10 nm Production 2016;
Outlook: 7 nm production in 2018, 5 nm 2020$

MCP, SiP, MCM,
3D Stacked Dice,
Heterogeneous
Integration
(Wirebond,
Flipchip, SMT)

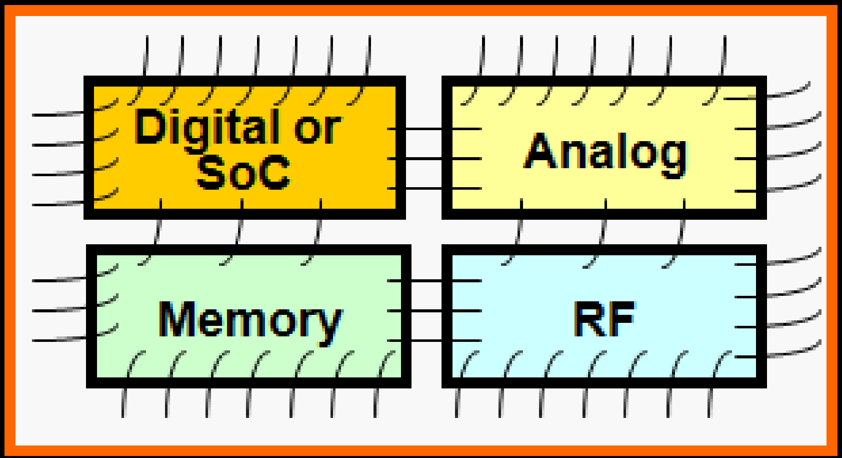
Fig. 5. A Sketch of Silicon Age 3.0 due to a Creative Volumetric-Scaling Methodology [6,7] and a 3D Wafer-based System Integration Achieving Form-Factor Scaling [9,11] to Create EME,), A-SSCC2016

Evolving System Chip Architectures

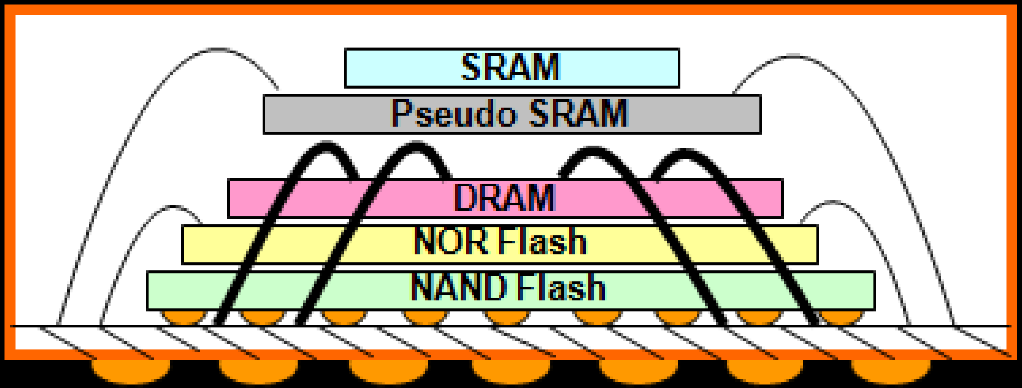
- **SoC** (System-on-a-Chip)



- **SiP** (System-in-Package)



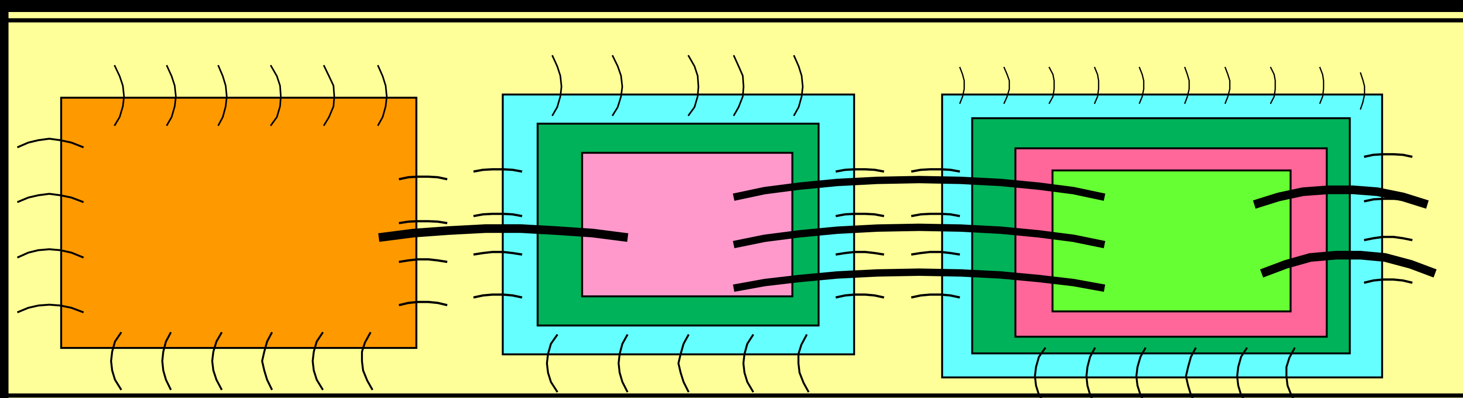
- **MCSP** (Multiple die stacking in Chip Scale Package)



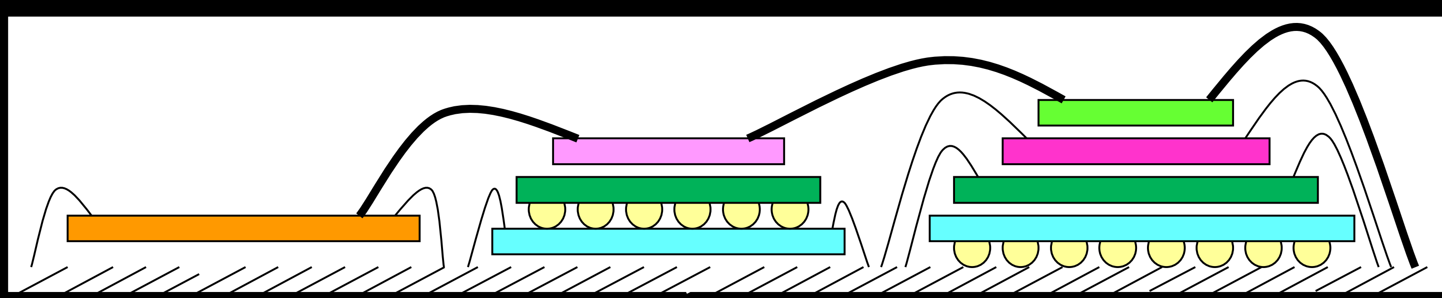
*After Nicky Lu, ISSCC 2004 Plenary Talk

Heterogeneous Integration (HI) Impacts Silicon3.0

- New System Architecture by Dice in a Package: Multi-Dimension Layout to Increase Integration instead of Simply Device Shrinkage
- mDIC (m-Dimensional Dice Integration Chip); m= 2, 2.5, 3, 4…



e.g. RF or Power | Analog or Cache over SoC | Memory + Logic



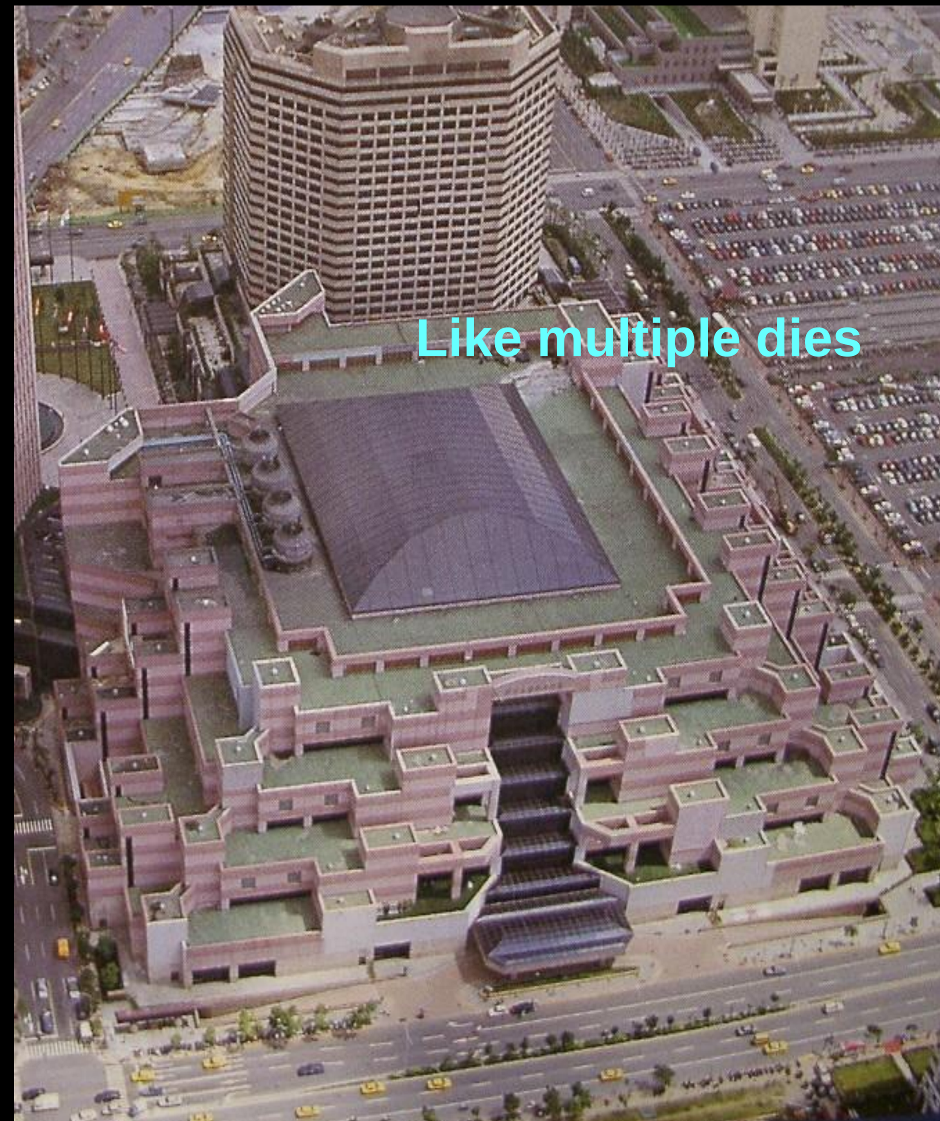
*After Nicky Lu, ISSCC 2004 Plenary Talk

MDICAnalogy

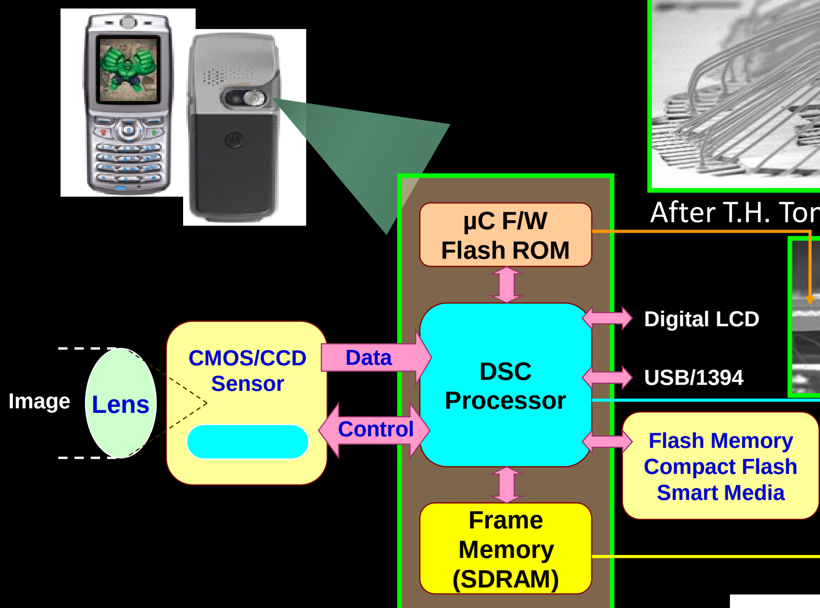
- **Metropolitan-like Die-Society IntegratedCluster**

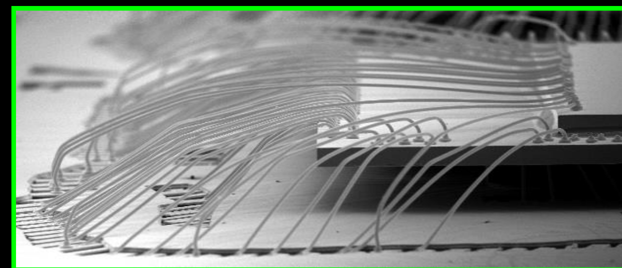
  e.g.Taipei World Trade Center versusone-story range at Texas

Like single die

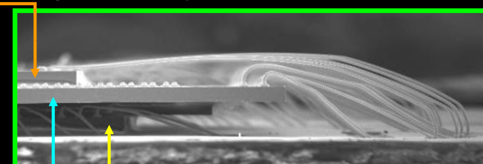


A Breakthrough in Si3.0 : Known-Good-Die Technology Enables Stacked-Die System-Chip

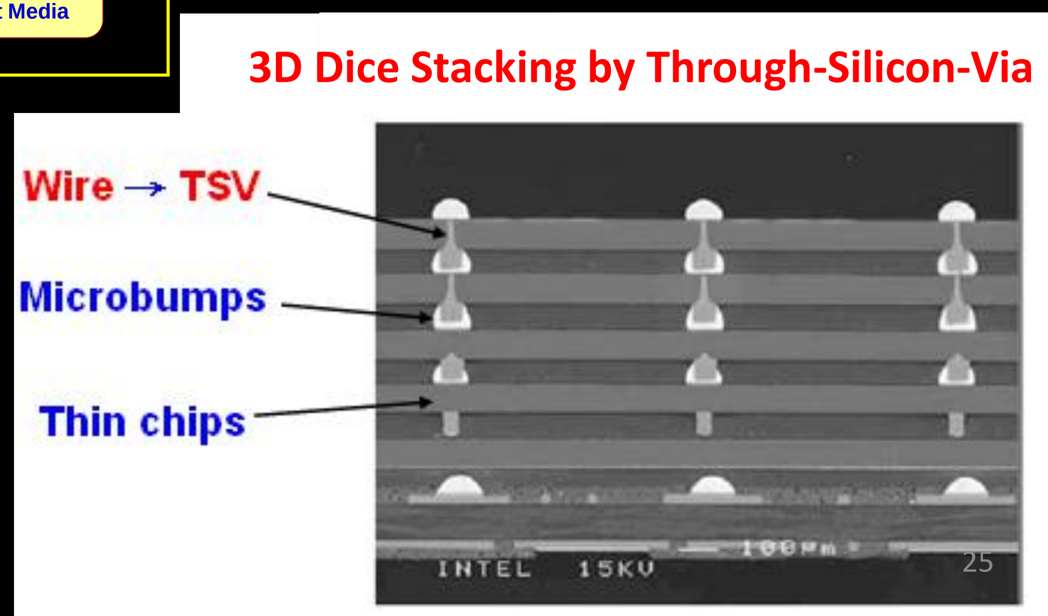




After T.H. Tong (ASE Corp.) ; N. Lu, ISSCC 2004



Etron Has Been Shipping KGD DRAM Since 2002. Shipments Have Totaled Over 1 Billion Units by 2015. This Has Made Etron Known as a Leading Contributor in 3D Technology

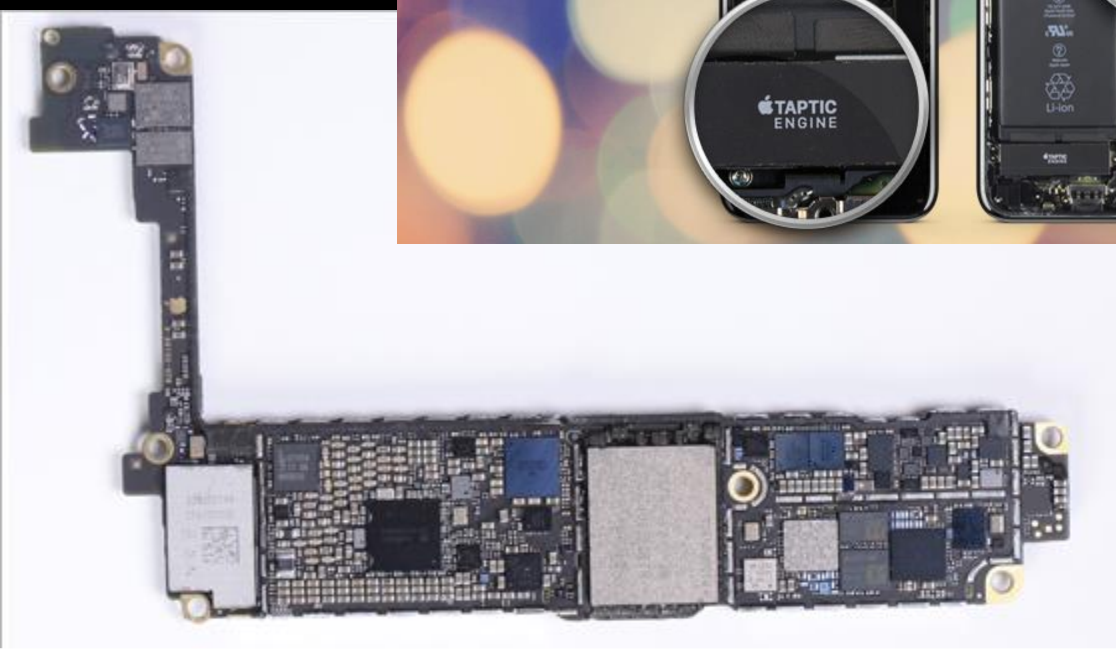


Intel's TSV (Through Silicon Via), 2013

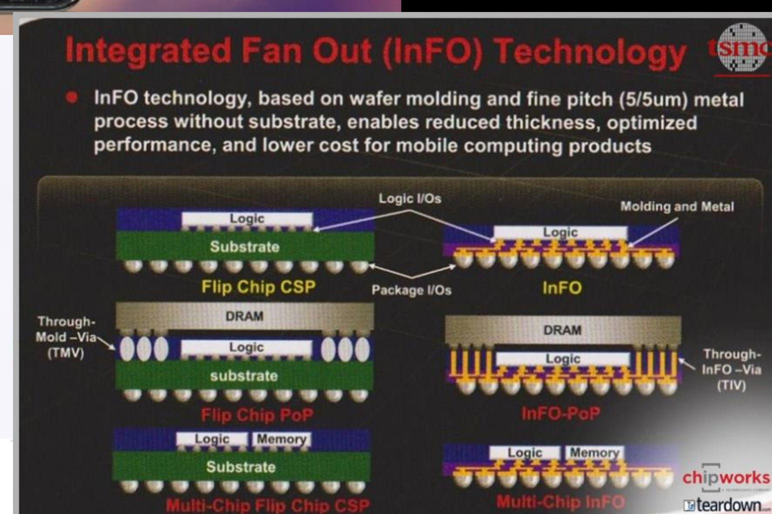
Latest HI Example：

3D Bare-Die+Chip+InFO inside iPhone 7

2016

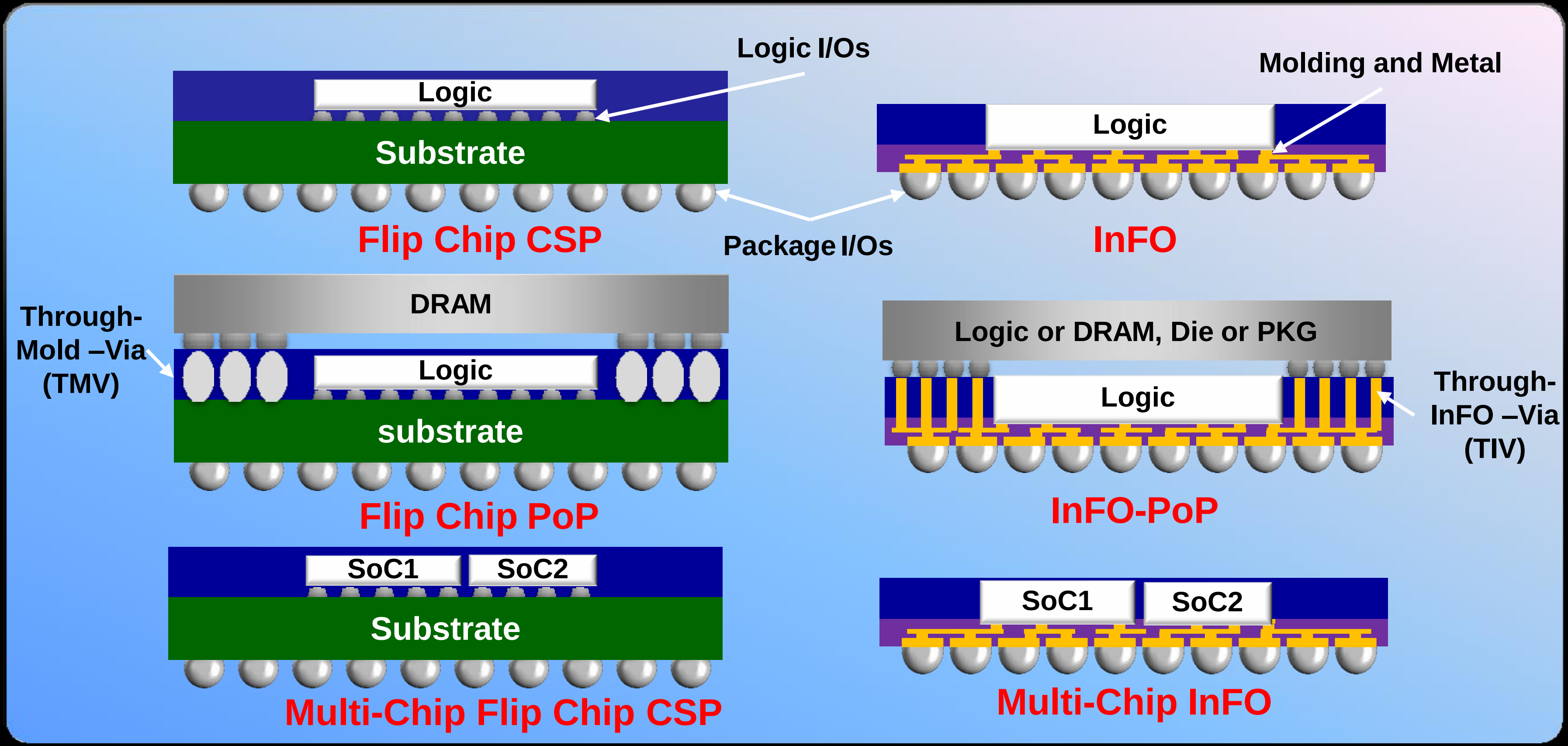


Source: Chipworks.com; September, 2016



TSMC's Integrated Fan-Out (InFO) Technology

- Based on Wafer Molding and Fine Pitch (5/5um) Metal Process without Substrate, Enables Reduced Thickness, Optimized Performance, and Lower Power and Cost for Mobile Computing Products



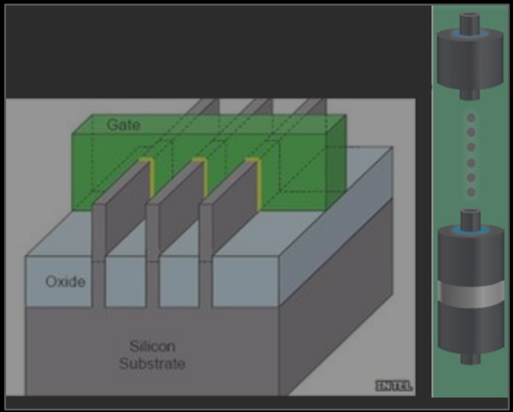
After Douglas Yu, July 2016

Another Volume-Scaling Method Is Happening and Enabling an Effective Moore's Law Economy (EME)

2D
Line
Scaling
(Planar)

→

3D Areal Density or
Area Scaling
3D FinFET+(>0.7X
Line Scaling) Continue
Moore's 2X Law



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10 nm Production 2016;
Outlook: 7 nm production in 2018, 5 nm 2020$

MCP, SiP, MCM,
3D Stacked Dice,
Heterogeneous
Integration
(Wirebond,
Flipchip, SMT)

→

3D Wafer-based
System Integration &
Form-Factor Scaling,
(CoWoS,
InFO-PoP, …)

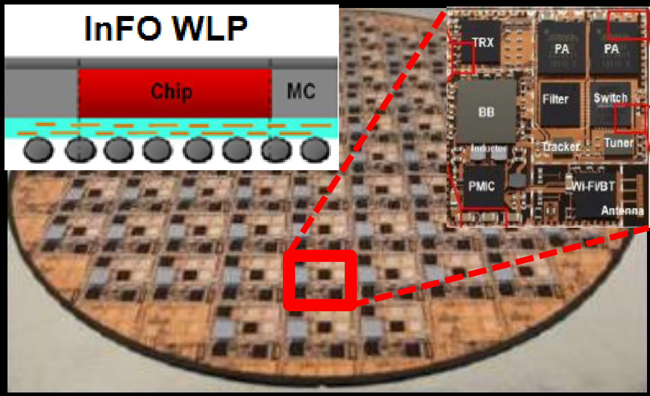
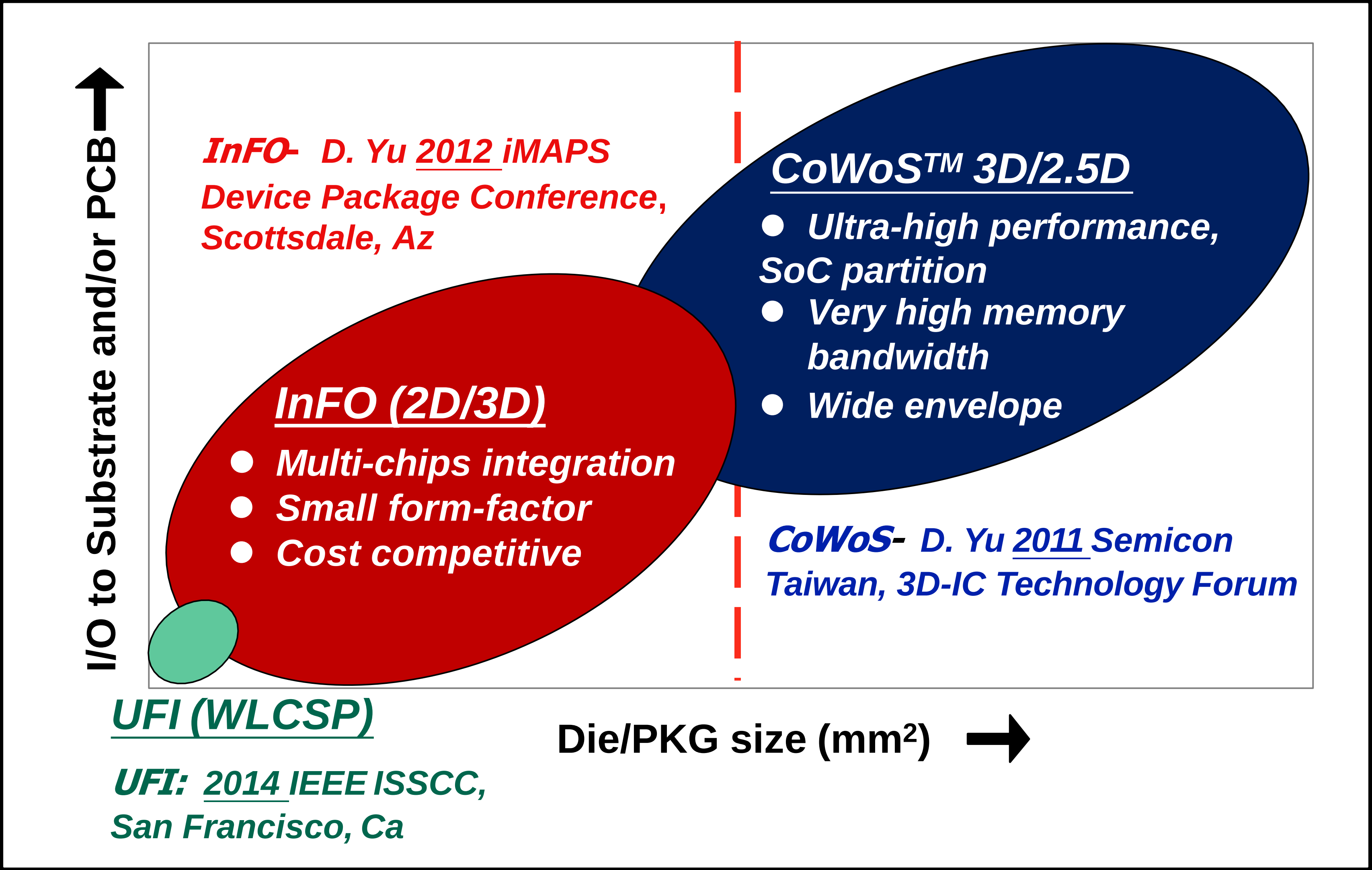


Fig. 5. A Sketch of Silicon Age 3.0 due to a Creative Volumetric-Scaling Methodology [6,7] and a 3D Wafer-based System Integration Achieving Form-Factor Scaling [9,11] to Create EME,), A-SSCC2016

TSMC's WLSI Technology Platform for HI Sets New Industry Trends



After Douglas Yu, July 2016

Now a Virtual Moore's Law Economy (VME) Is Being Incubated by Function X Value Scaling with Heterogeneous Integration (HI)

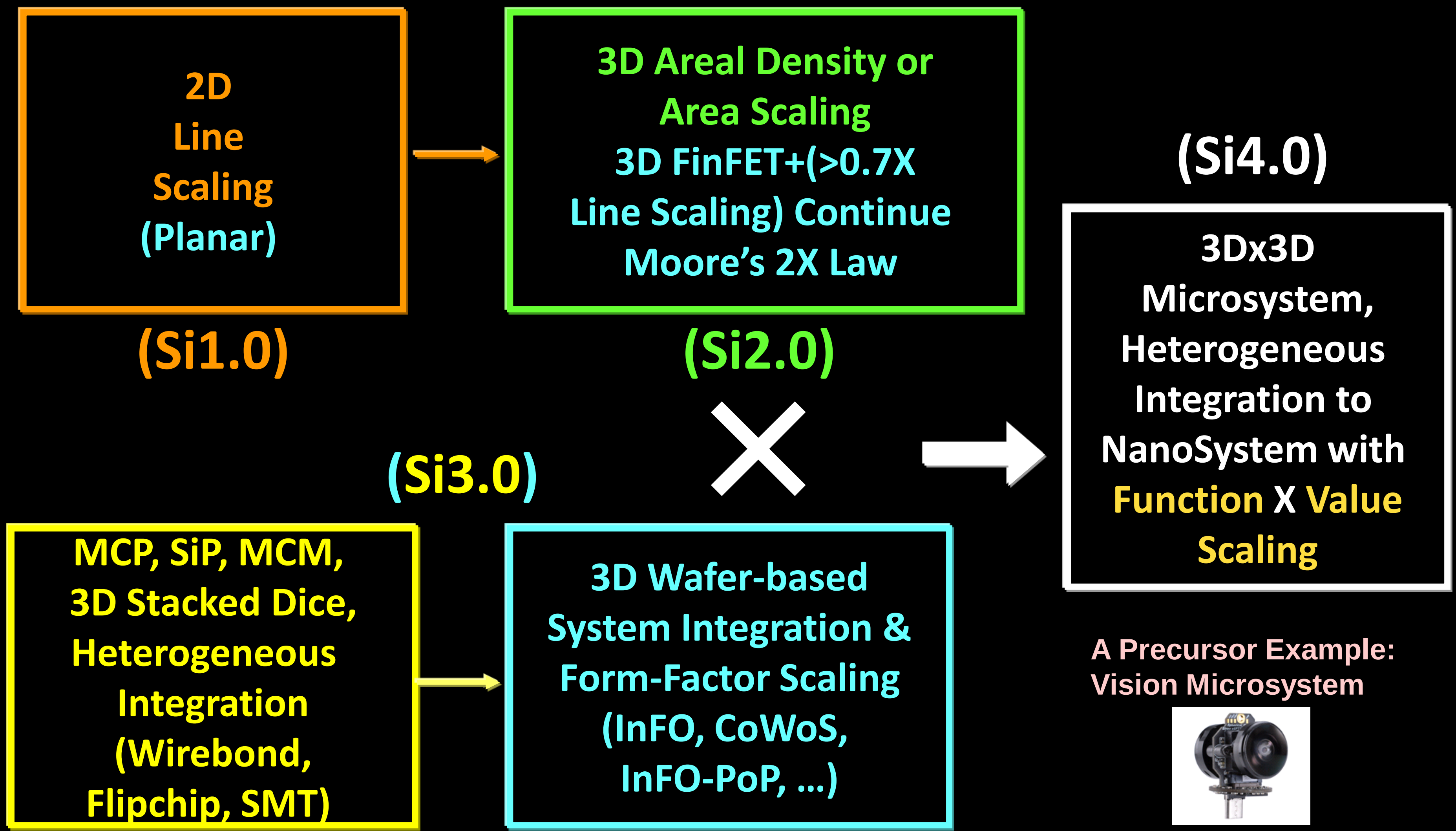


Fig. 6. An Illustration on the Roadmap toward Future 3Dx3D [9] Heterogeneous Integrated Nano-system for Enlarging Silicon Values with a (Function X Value)-Scaling Methodology to Create VME (Silicon Age 4.0), A-SSCC2016

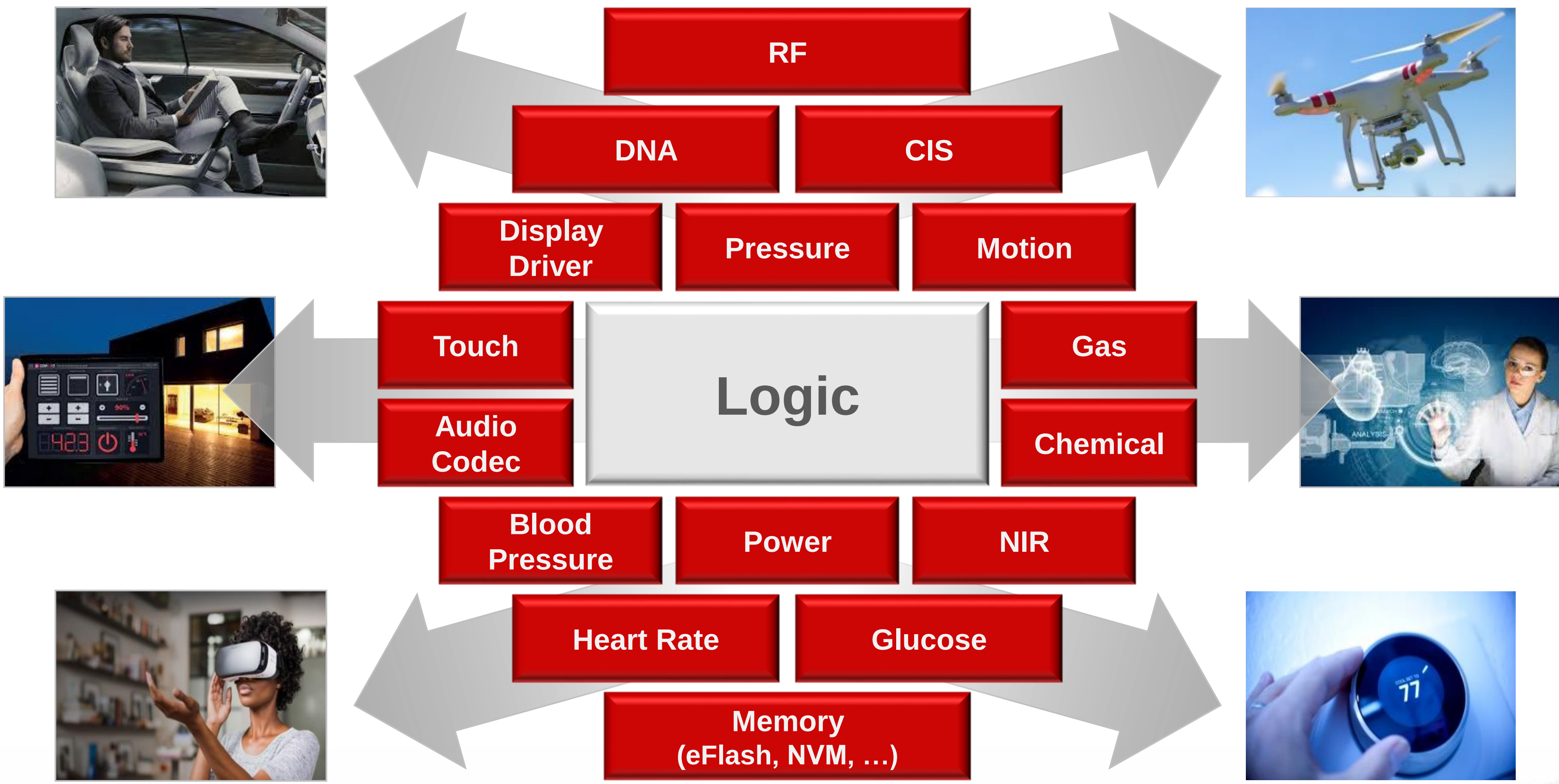
LyfieEye™：A New Way of Capturing Selfie and Life's Important Moments in Spherical 360˚ Videos

Source: [16] A Spherical 360˚ Video Capture Micro-system as LyfieEye (Selfie+Life), eCapture Technologies, Inc., USA

Capturing the Full World Around You –
Whenever & Wherever You Control Whatever to Watch

TSMC Property

Heterogeneous Technology Integration for More Functionality



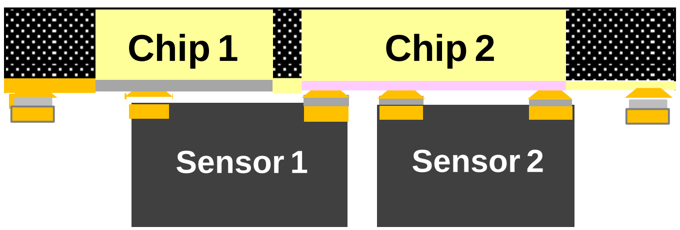
Source: Mark Liu, TSIA Annual Convention, September 29, 2016

TSMC Property

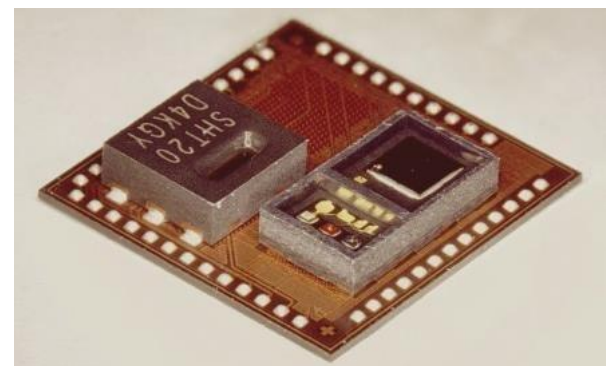
Compact 3D-Stacking Realizes Intelligent Systems

Multi-chips, multi-sensors intelligent systems

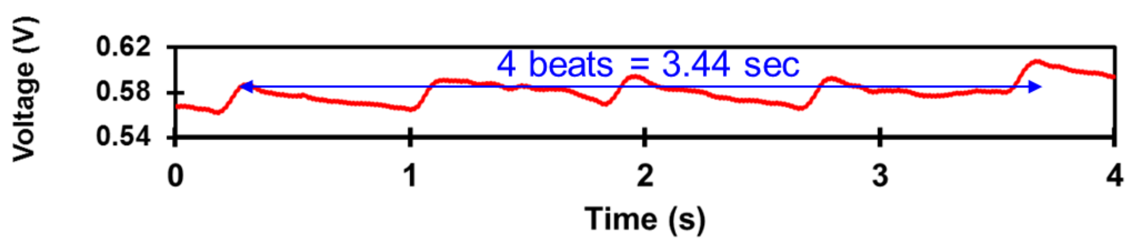
Scheme



Intelligent System



Heart Rate Sensor



Pulse Rate: 4/3.44x60 = 70 (beats/min)

Source: Douglas Yu, July 2016

Heterogeneous Integration

Enabling the future of the Electronics Industry

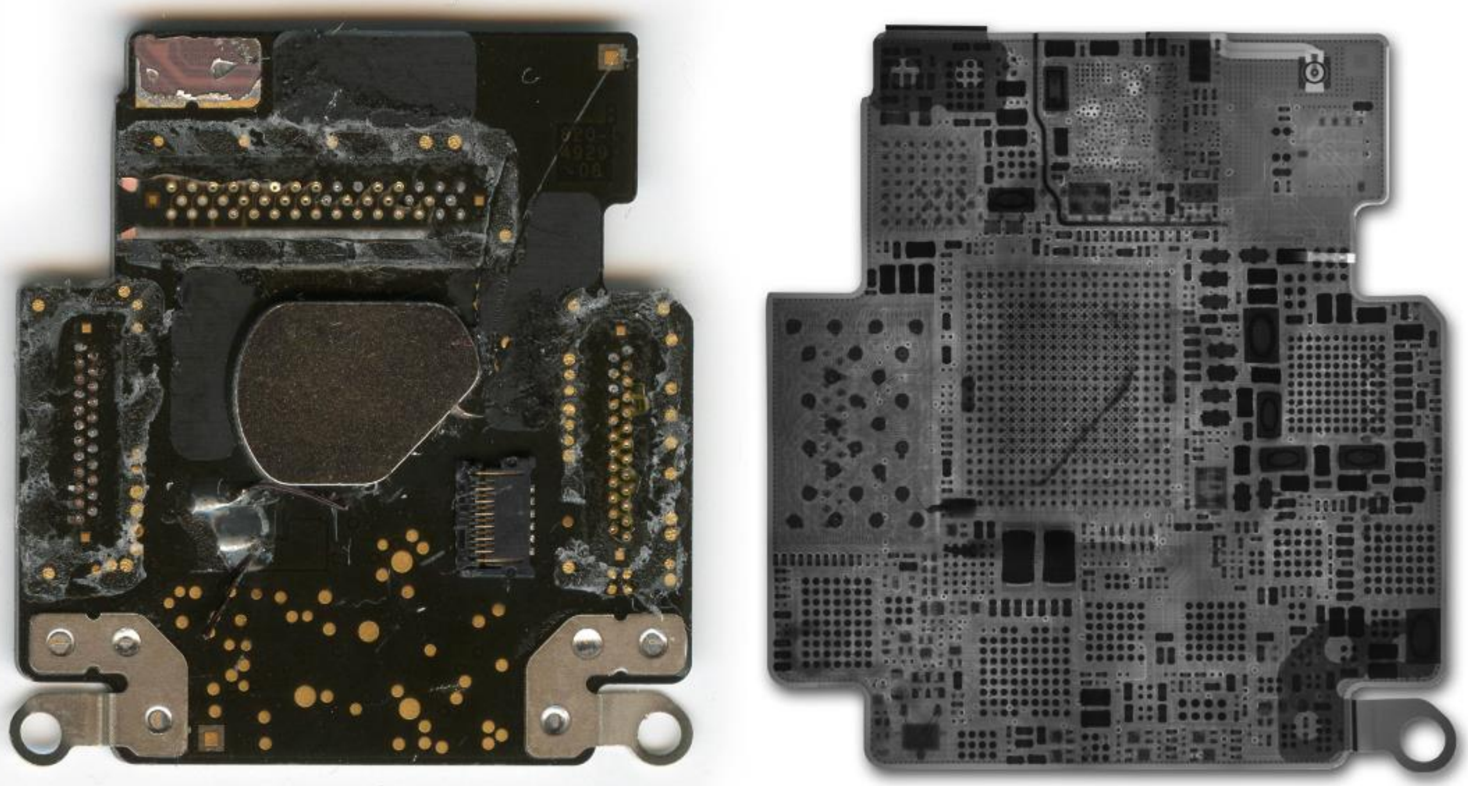
Presented by W. R. Bottoms PhD

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

After W. Bottoms, Aug.12 2016

Apple Watch S1 : An HI Example

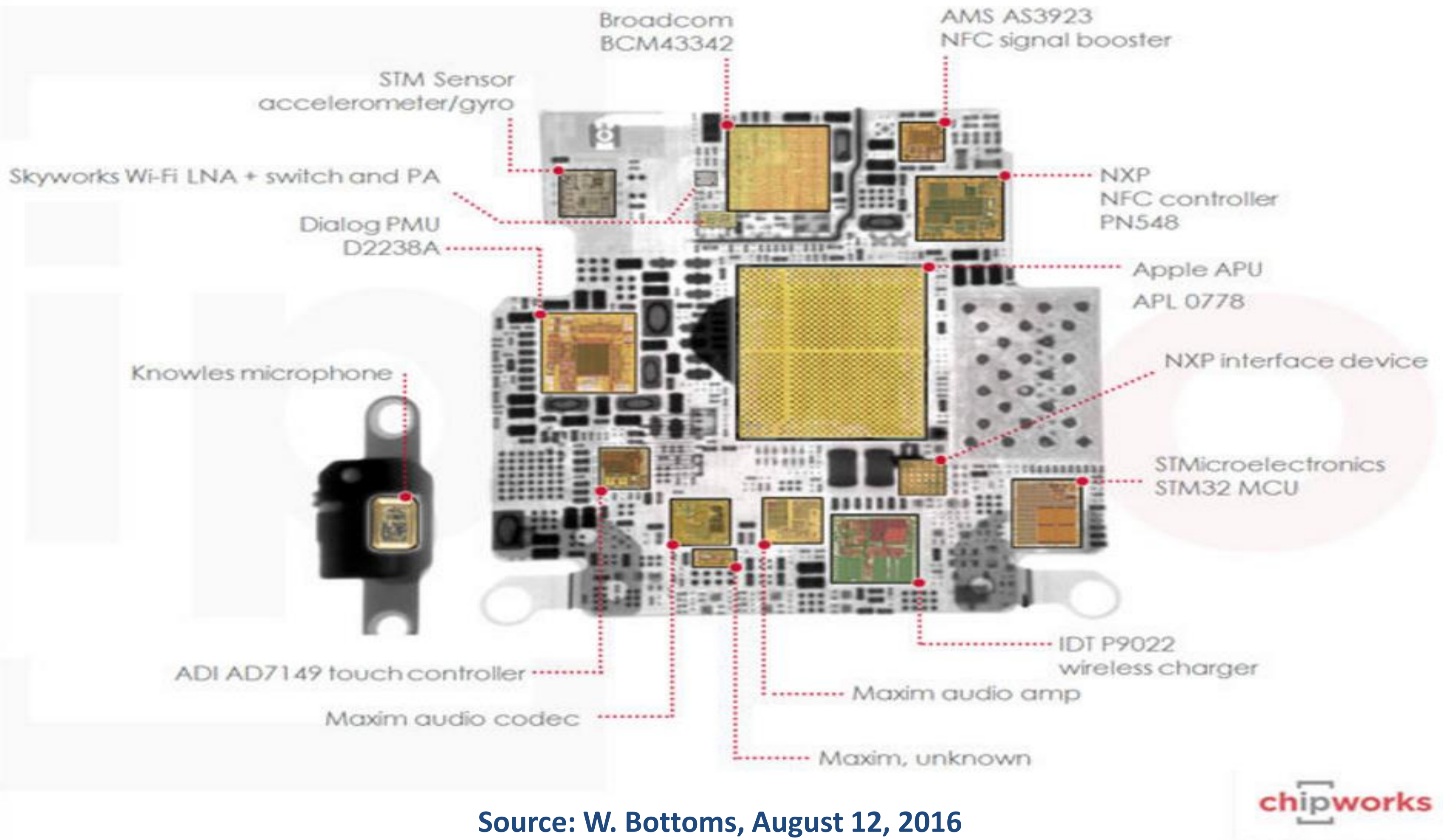
Complex, high performance, low cost and this is just the beginning



Source: W. Bottoms, August 12, 2016

Apple Watch S1 : An HI Example

Complex, high performance, low cost and this is just the beginning

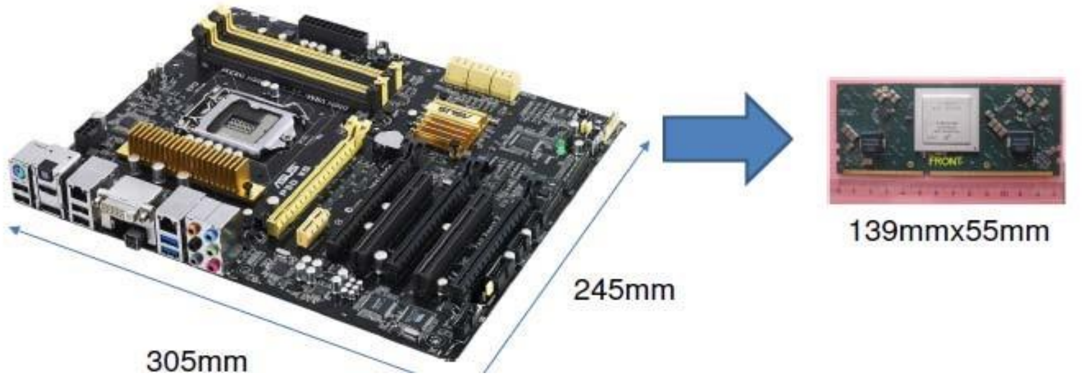


Source: W. Bottoms, August 12, 2016

Micro-server Packaging Can Enable Power, Cost and Performance Gains

- ✓ the Comparison with Standard Product Is Dramatic Even with Conventional PCB Assembly and Standard Off-the-Shelf Components (Freescale T4240)
- ✓ Small Size Allows Photonics to Remain at Rack Unit Edge

40% faster with 70% of Intel Xeon E3-1230l power yields 2X the operations per watt



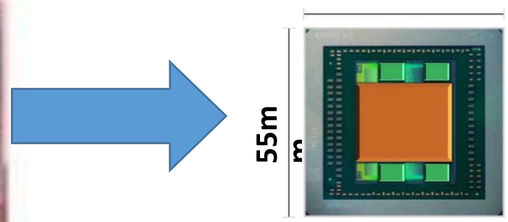
Source: Ronald P. Luijten MIT workshop 7/28/2015

Source: W. Bottoms, August 2016

What Could We Do with 3D Packaging?

- ✓60% smaller with 16Gb high bandwidth memory
- ✓4096 bit memory interface
- ✓512GB/s memory bandwidth
- ✓Si interposer with **TSV & μbump** to package substrate
- ✓Lower power
- ✓22 discrete die plus passive components

139mmx55mm

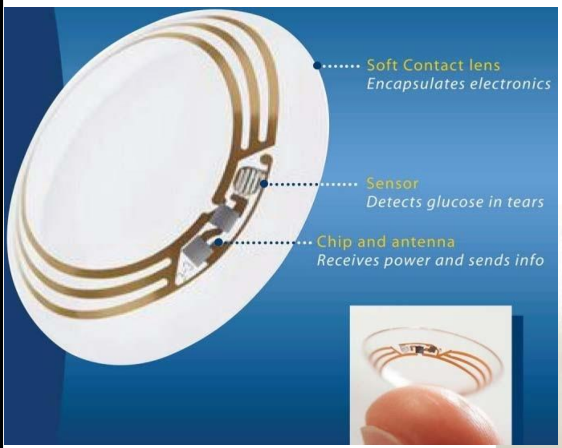


592mm^2 ASIC
1011mm^2 interposer

Source: W. Bottoms, August 2016

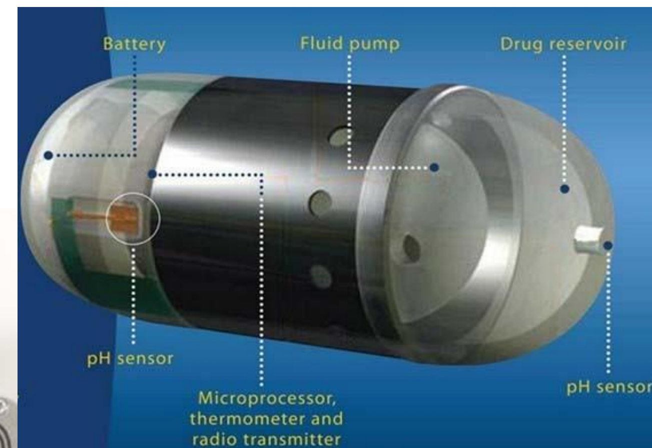
An Unlimited Number of IoT Products Emerging

Wearable concussion sensor
concussion history
power management
motion sensor Radio



Wireless glucose sensor for diabetics

Frying pan controlled by smartphone app.



Robotic Drug delivery
Pill swallowed by Patient

Source: W. Bottoms, August 2016

MDSC Design/Technology Challenges

- **Connect Knowledge of ICs with Electronic Systems**
- **Optimization of Design across System, Software, Fab Process, Packaging and Testing Segments**
  - Known-Good-Die technologies: reliability and cost;
  - Multi-layer interconnected substrates with passives;
  - Micro-assembly: wafer thinning, die stacking, flip-chip or
  - wire bonding either to substrate or die to die, encapsulation;
  - Signal integrity: inter-die, intra-die, chip interface;
  - Supply voltage management and power control;
  - Simulations: die-to-die, die-to-package, package-to-field;
  - Testing/verification of multiple circuit family behaviors;
  - Error correction, reparability, programmability;
  - Development challenges from GigaScale to TeraScale, etc.

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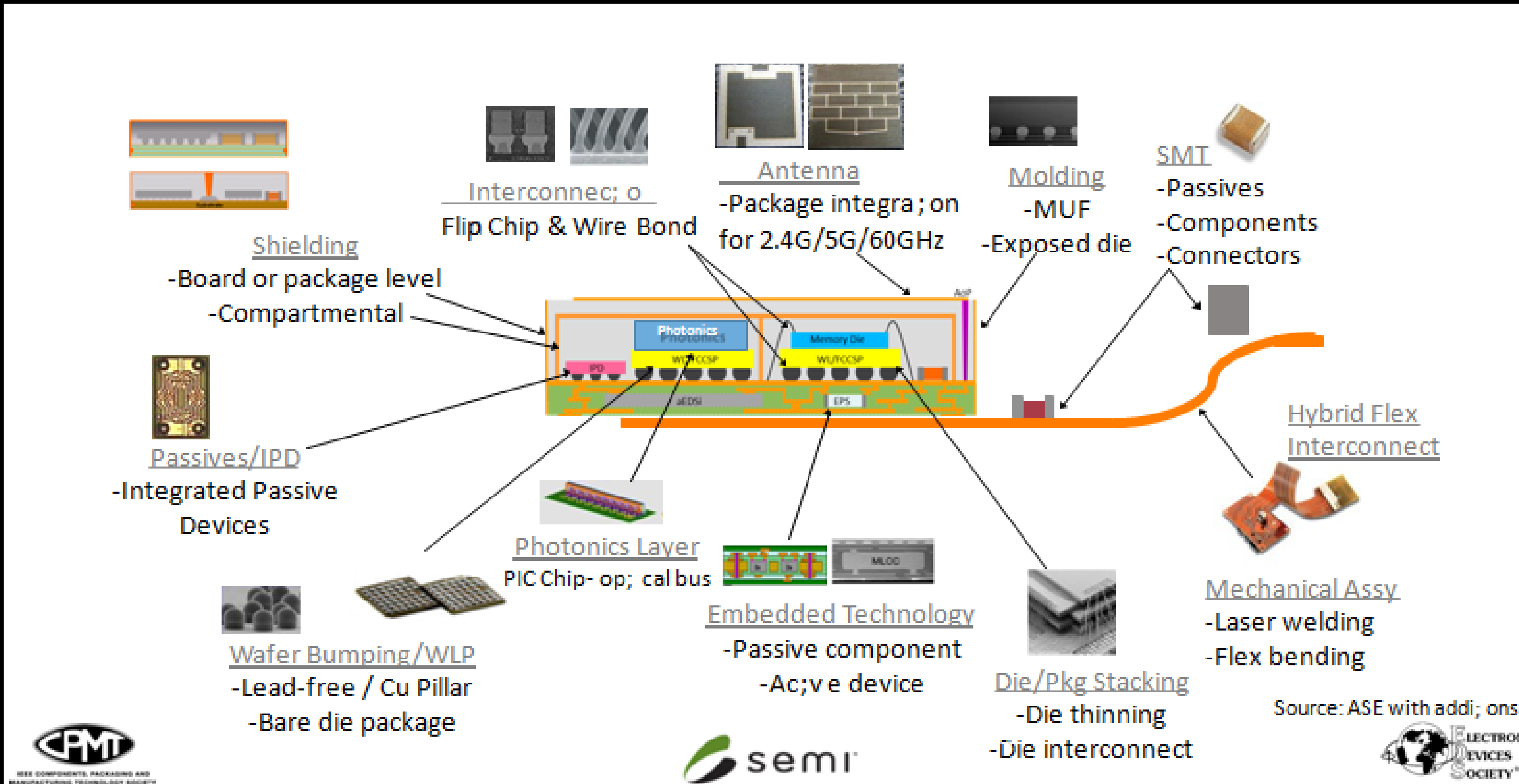
A Very Tough Challenge Is How to Reduce Power and to Facilitate Thermal Dissipation !

HIDAS : Heterogeneous Integrated Design/Architecture/ System for Silicon-Centric Nano-System in Si4.0

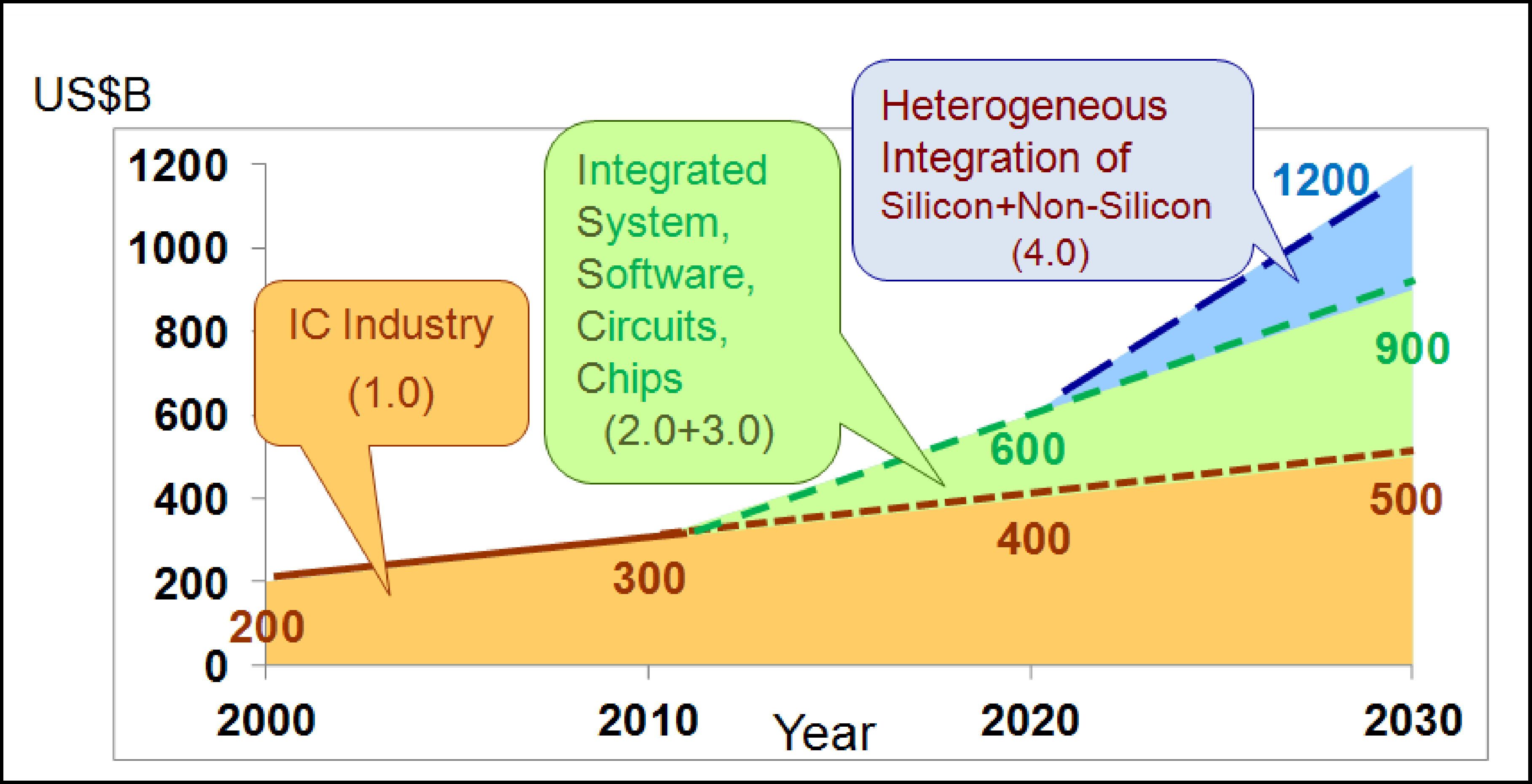
- New Vertical Design/Method for Future Chip Design Covering Holistically from Final System-Product, IC Design Deep Down to Device Level
- System-Performance Optimized by a HIArchitecture to Holistically Synthesize Merits from Physics, Materials, Devices, Circuits, Software, Systems for Application Needs
- New VME Way : eg. a 5nm CMOS Base, 1nm Carbon-Nano-Tube MoS_2 for Critical-path Performance [15], KGDM or MRAM, InFO, RF/Analog Dice, DRAM Chips, Image or Pressure Sensors, MEMS or Micro-Lenses Stacked on TiVs, Bottom PCBs with Heat-Sinks, etc. in an Effective 1nm Silicon-Centric HI Product Delivering High Function & Values for Justifying ROI as Needed to Be Catalysts in the VME (Virtual Moore's Law Economy) Era
- Line/Area/Volume-Scaling Down + FunctionXValue Scaling Up

Electronic/Photonic SiP through Heterogeneous Integration (HI)



Source: William (Bill) Chen, August 2016

A Sketch of Future Silicon Economy Potential Due to Many Silicon-Intelligence Applications Being Created by HI-VME

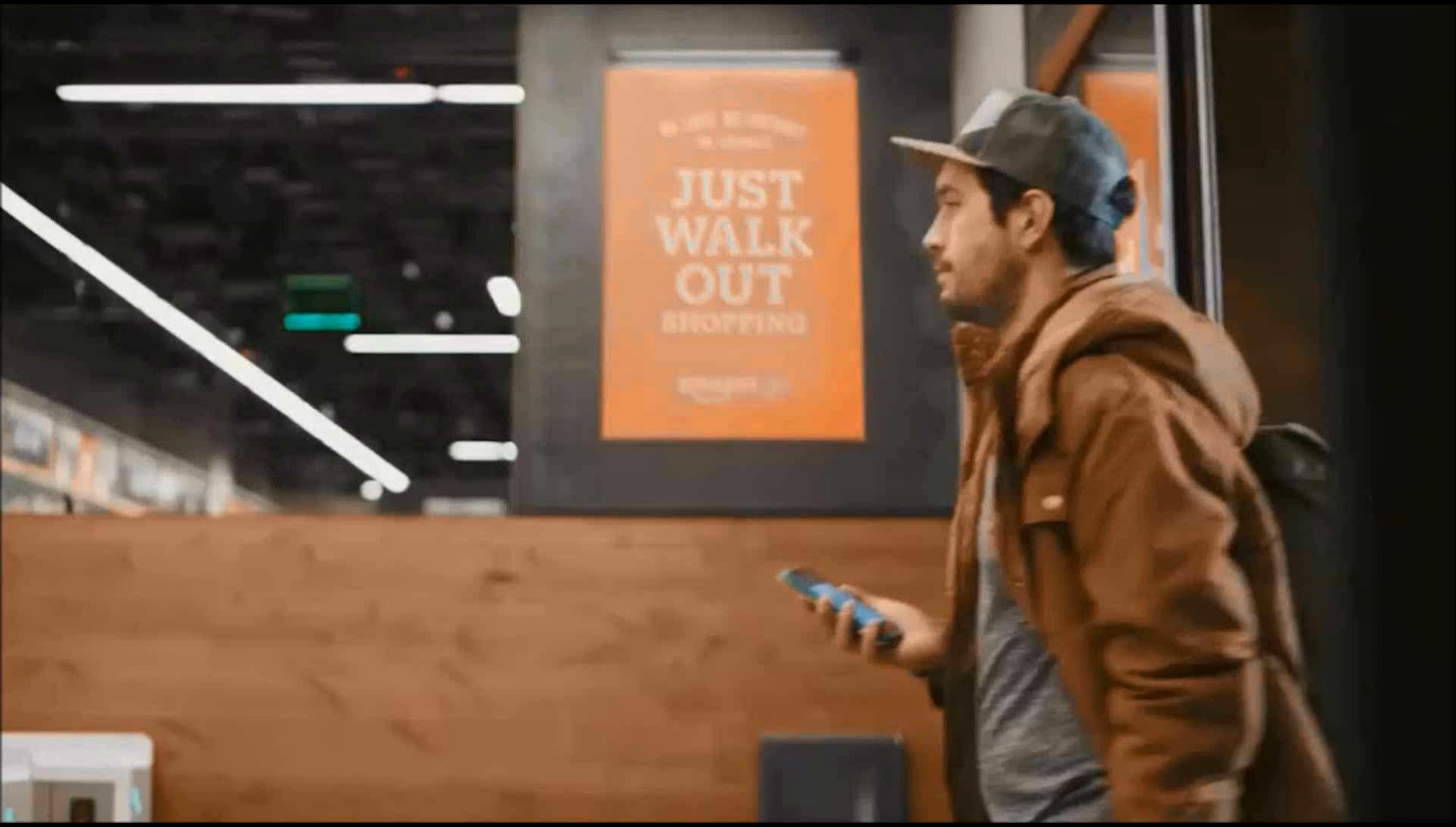


An Emerging Transformative Revolution in 21st Century

- A Revolution Driven by Diverse&Boundless Smart Applications Enabled by Science& Technology Advancement
  - Many Ways of Artificial and Machine Intelligences
  - Power Stems from Integrated Circuits, Algorithm, System & Software
  - Computerized DNA/Cell/Microbiome Personalized Medicine for Longer Life

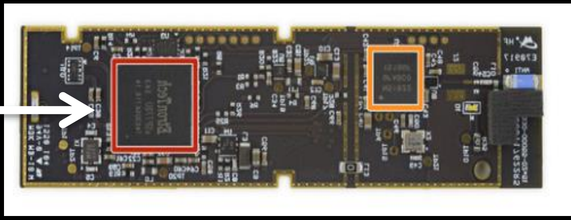
Innovative Convenience Store Shopping –
"Just Walk Out" Technology

Technology's Diverse and Boundless Applications (Example IV)



VR / AR Application：Oculus Rift & Touch

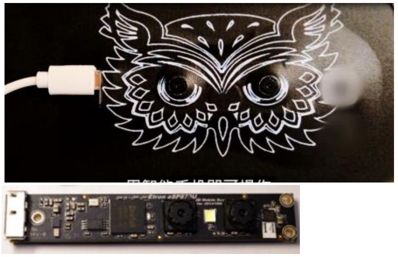
Etron’s 3D Depth Map Chip



AI Vision :

Natural Vision vs Computer Vision

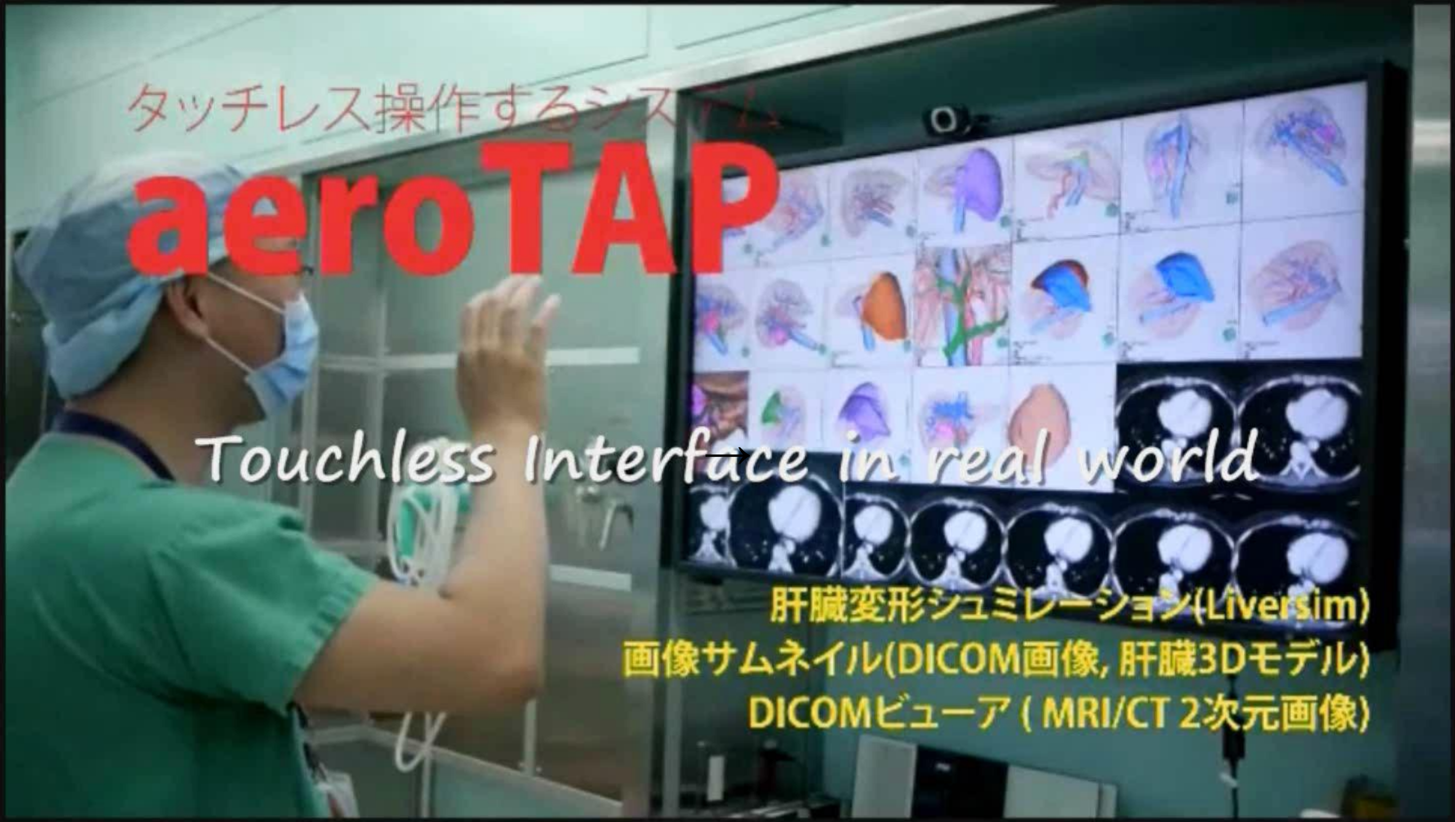
3D Depth Map IC & Platform



Etron's 3DStereoscoping Product , CES '17

Robot-Eye Solution for Industry 4.0

AI Vision for Medical Usage:Touchless Technology in Surgery



IC Chip Original Design →

Compact Module →

Etron's Cyber 6dEye

AI inside PI：Pervasive Intelligences*

- Natural Human Intelligence
- Artificial Intelligence & Machine-Robotic-Human Symbiotic/Synergetic Intelligence
- Living & Life Intelligence
- Society & Humanity Intelligence

* Created by Nicky Lu and Prof. Jason Wang (Stanford Medical School)

Conclusion

- **IC Line-Scaling Methodology Created ME (Moore's Law Economy)**
  - **From 30µm to 32/28nm; One to 10^8 transistors per mm^2 silicon area**
- **Creative Area-Scaling and Volume-Scaling Methodologies Have Extended ME to Today's EME (Effective Moore's Law Economy)**
  - **28/22 down to 10/7nm; 3D Transistor and 3D NAND**
- **Emerging Function X Value Scaling Methodology Utilizing Heterogeneous Integration (Silicon-only or Silicon+Non-Silicon)**
  - **Empower smart Nano-systems with higher value and enhance productivity per silicon-IC area, creating many new applications with lower power/cost and higher performance, resulting in strong ROI for VME (Virtual Moore's Law Economy)**
  - **From 7nm toward 5.0, 3.5, 2.5, 1.8, 1.0-nm nodes by using a new function x Value Scaling Down & Up Rule**
  - **VME continues IC industry growth by effectively increasing Nano-systems' Dollar-amount per area induced by HIArchitecture with HIDAS design methods**

Thank You!