CALL FOR PAPERS

ISLPED 2017

INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

http://www.islped.org
Taipei, Taiwan
July 24 – 26, 2017

Information: islped@islped.org
Follow us on Twitter: @islped

Organizing Committee and Symposium Officers:

General Co-Chairs
Chia-Lin Yang, NTU
yangc@csie.ntu.edu.tw

David Garrett, Broadcom
garrettd@broadcom.com

Program Co-Chairs
Thomas Wenisch, Univ. Michigan
twenisch@umich.edu

Jaydeep Kulkarni, Intel
jaydeep.p.kulkarni@intel.com

Publicity Co-Chairs
Jae-Joon Kim, POSTECH
jaejoon@postech.ac.kr

Umit Ogras, ASU
umit@asu.edu

Treasurer
Yi-Jung Chen, NCNU
yjchen@ncnu.edu.tw

Web Chair
Hsiang-Yun Cheng, Sinica
hycheng@citi.sinica.edu.tw

Industry Liaisons
John Redmond, Broadcom
jcredmon@broadcom.com

Tai-Cheng Lee, NTU
tlee@ntu.edu.tw

Tsung-Yi Ho, NTHU
tyho@cs.nthu.edu.tw

Publication Chair
Iris Hui-Ru Jiang, NCTU
huiru.jiang@gmail.com

Local Arrangement Co-Chairs
Pi-Cheng Hsiu, Sinica
pchsiu@iis.sinica.edu.tw

Yuan-Hao Chang, Sinica
johnson@iis.sinica.edu.tw

Registration Chair
Tsung-Te Liu, NTU
ttliu@ntu.edu.tw

Design Contest Co-Chairs
Saibal Mukhopadhyay, Georgia Tech
saibal@ece.gatech.edu

Yongpan Liu, NTHU
ypliu@tsinghua.edu.cn

Pending sponsorship by the **ACM Special Interest Group on Design Automation (SIGDA)** and the **IEEE Circuits and Systems Society (CASS)**.

The International Symposium on Low Power Electronics and Design (ISLPED) is the premier forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, system-level design and optimization, to system software and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

1. Technology, Circuits, and Architecture	2. CAD, Systems, and Software
1.1. Technologies Low-power technologies for Device, Interconnect, Logic, Memory, 2.5/3D, Cooling, Harvesting, Sensors, Optical, Printable, Biomedical, Battery, and Alternative energy storage devices.	**2.1. CAD Tools and Methodologies** CAD tools and methodologies for low-power and thermal-aware design addressing power estimation, optimization, reliability and variation impact on power, and power-down approaches at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.
1.2. Circuits Low-power digital circuits for Logic, Memory, Reliability, Clocking, Power gating, Resiliency, Near-threshold and Sub-threshold, Variability, and Digital assist schemes; Low-power analog/mixed-signal circuits for Wireless, RF, MEMS, AD/DA Converters, I/O, PLLs/DLLS, Imaging, DC-DC converters, and Analog assist schemes.	**2.2. Systems and Platforms** Low-power, power-aware, and thermal-aware system design including data-center power delivery and cooling, platforms for SoCs, embedded systems, approximate and brain-inspired computing, the Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability.
1.3. Logic and Architecture Low-power logic and microarchitecture for SoC designs, Processor cores (compute, graphics and other special purpose cores), Cache, Memory, Arithmetic/Signal processing, Cryptography, Variability, Asynchronous design, and Non-conventional computing.	**2.3. Software and Applications** Energy-efficient, energy-aware, and thermal-aware software and application design including scheduling and management, power optimizations through HW/SW interactions, and emerging software low-power applications.

3. Industrial Design Track

ISLPED'17 solicits papers for an "Industrial Design" track to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics, but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs. Industrial design papers that focus on any of the topics mentioned in the tracks above are welcome.

Submissions on new topics: emerging technologies, architectures/platforms, and applications are particularly encouraged.

Technical Paper Submission Deadlines: Abstract registration by ~~Feb 27~~ Mar 6, 2017, at 11:59pm Pacific Standard Time
Full paper due by ~~Mar 6~~ Mar 13, 2017, at 11:59pm Pacific Standard Time
Invited Talk, Panel, and Embedded Tutorial Proposals Deadline: April 16, 2017
Notification of Paper Acceptance: May 3, 2017
Submission of Camera-Ready Papers: June 1, 2017

Submissions should be full-length papers of **up to 6 pages** (PDF format, double-column, US letter size, using the IEEE Conference format, available at http://www.ieee.org/conferences_events/conferences/publishing/templates.html), including all illustrations, tables, references, and an abstract of no more than 250 words. **Submissions must be anonymous**. Submissions exceeding 6 pages or identifying the authors, either directly or through explicit references to their prior work, will be automatically rejected. More information about paper submission can be found at http://www.islped.org.

Submitted papers must describe original work that has not been published/accepted or currently under review by another journal, conference, symposium, or workshop at the same time. Accepted papers will be submitted to the IEEE Xplore Digital Library and the ACM Digital Library. ISLPED'17 will present two Best Paper Awards based on the ratings of reviewers and a panel of judges.

There will be several invited talks by industry and academic thought leaders on key issues in low power electronics and design. The Symposium may also include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions in low power electronics and design. Proposals for invited talks, embedded tutorials, and panels should be sent by email to the ISLPED'17 Technical Program Co-Chairs, Jaydeep Kulkarni (jaydeep.p.kulkarni@intel.com) and Thomas Wenisch (twenisch@umich.edu) by the deadline listed above.

Participants interested in exhibiting at the Symposium should contact the General Co-Chairs by May 1, 2017.