

Monday, July 24

7:30	Breakfast (continues until 9:00)	
08:00 – 08:40	Conference Registration	
08:40 – 09:00	Welcome by General and Program Co-Chairs [Forum Hall]	
09:00 – 10:00	<p style="text-align: center;">Keynote I A New Silicon Age 4.0: Generating Semiconductor-Intelligence Paradigm with a Virtual Moore's Law Economics and Heterogeneous Technologies <i>Dr. Nicky Lu</i> <i>Etron Technology, Inc.</i></p> <p style="text-align: center;">Chair: <i>Chia-Lin Yang (National Taiwan University)</i> [Forum Hall]</p>	
10:00 – 10:30	Coffee Break	
10:30 – 11:45	<p style="text-align: center;">Session 1A Memories & their Applications</p> <p style="text-align: center;">Session Chair: <i>Sangyoung Park (TU München)</i> [Locke Hall]</p>	<p style="text-align: center;">Session 1B Design Implications of Novel Interconnects & Technologies</p> <p style="text-align: center;">Session Chair: <i>Alper Buyuktosunoglu (IBM T.J. Watson Research Center)</i> [Archimedes Hall]</p>
	<p>Write-Energy-Saving ReRAM-Based Nonvolatile SRAM with Redundant Bit-Write-Aware Controller for Last-Level Caches <i>Tsai-Kan Chien^{1,2}, Lih-Yih Chiou¹, Yi-Sung Tsou¹, Shyh-Shyuan Sheu², Pei-Hua Wang², Ming-Jinn Tsai² and Chih-I Wu²</i> ¹National Cheng Kung University, ²Industrial Technology Research Institute</p> <p>Charge Recycled Low Power SRAM with Integrated Write and Read Assist, for Wearable Electronics, Designed in 7nm FINFET</p>	<p>A Carbon Nanotube Transistor based RISC-V Processor using Pass Transistor Logic <i>Best Paper Nominee</i> <i>Aporva Amarnath, Siying Feng, Subhankar Pal, Tutu Ajayi, Austin Rovinski and Ron G. Dreslinski</i> <i>University of Michigan</i></p> <p>Architecting Large-Scale SRAM Arrays with Monolithic 3D Integration <i>Joonho Kong¹, Young-Ho Gong² and Sung Woo Chung²</i> ¹Kyungpook National University, ²Korea University</p>

	<p>Technology <i>Vivek Nautiyal, Gaurav Singla, Satinderjit Singh, Fakhruddin ali Bohra, Jitendra Dasani, Lalit Gupta and Sagar Dwivedi</i> ARM, Ltd.</p> <p>Spin-Torque Sensors with Differential Signaling for Fast and Energy Efficient Global Interconnects <i>Zubair Azim and Kaushik Roy</i> Purdue University</p>	<p>Temporal Codes in On-Chip Interconnects <i>Michael Mishkin¹, Nam Sung Kim² and Mikko Lipasti¹</i> ¹University of Wisconsin-Madison, ²University of Illinois Urbana-Champaign</p>
11:45 – 13:00	<p>Lunch [2F Just Italian, Just Sleep]</p>	
	<p>Poster Session</p> <p>Session Chair: <i>Thomas Wensch (University of Michigan)</i> [Plato Hall]</p>	<p>Design Contest</p> <p>Session Chairs: <i>Saibal Mukhopadhyay (Georgia Tech), Yongpan Liu (Tsinghua University)</i> [Plato Hall]</p>
13:00 – 14:30	<p>Enabling Efficient Fine-Grained DRAM Activations with Interleaved I/O <i>Chao Zhang and Xiaochen Guo</i> Lehigh University</p> <p>Gabor Filter Assisted Energy Efficient Fast Learning Convolutional Neural Networks <i>Syed Shakib Sarwar, Priyadarshini Panda and Kaushik Roy</i> Purdue University</p> <p>Low Design Overhead Timing Error Correction Scheme for Elastic Clock Methodology <i>Sungju Ryu, Jongeun Koo and Jae-Joon Kim</i> Pohang University of Science and Technology</p>	<p>A Low-Power Dual-Core Motion Estimation Chip Design and Implementation for a Wireless Panoramic Endoscopy <i>Tsung-Yi Wu and Ching-Hwa Cheng</i> Feng Chia University</p> <p>An Atomic-Aware Design to Maximize Energy Utilization on NVP-based Self-Powered Sensor Systems <i>Chih-Kai Kang¹, Chun-Han Lin² and Pi-Cheng Hsiu¹</i> ¹Academia Sinica, ²National Taiwan Normal University</p> <p>High Energy-Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications</p>

	<p>Efficient Query Processing in Crossbar Memory <i>Mohsen Imani, Saransh Gupta, Atl Arredondo and Tajana Rosing UC San Diego</i></p> <p>A Low Power Duobinary Voltage Mode Transmitter <i>Ming-Hung Chien, Yen-Long Lee, Jih-Ren Goh and Soon-Jyh Chang National Cheng Kung University</i></p> <p>A Simple Yet Efficient Accuracy Configurable Adder Design <i>Wenbin Xu¹, Sachin Sapatnekar² and Jiang Hu¹</i> ¹Texas A&M University, ²University of Minnesota</p> <p>E-Spector: Online Energy Inspection for Android Applications <i>Chengke Wang, Yao Guo, Peng Shen and Xiangqun Chen Peking University</i></p> <p>A Case for Efficient Accelerator Design Space Exploration via Bayesian Optimization <i>Brandon Reagen¹, José Miguel Hernandez-Lobato², Robert Adolf¹, Michael Gelbart³, Paul Whatmough¹⁴, Gu-Yeon Wei¹ and David Brooks¹</i> ¹Harvard University, ²University of Cambridge, ³University of British Columbia, ⁴ARM Research</p> <p>SceneMan: Bridging Mobile Apps with System Energy Manager via Scenario Notification <i>Li Li¹, Jun Wang², Xiaorui Wang¹, Handong Ye² and Ziang Hu²</i> ¹Ohio State University, ²Huawei Technologies</p>	<p><i>Shouyi Yin, Peng Ouyang, Shibin Tang, Fengbin Tu, Xiudong Li, Leibo Liu and Shaojun Wei Tsinghua University</i></p> <p>An Ultra-Low Power 169-nA 32.768-kHz Fractional-N PLL <i>Chun-Yu Lin, Tun-Ju Wang, Tzu-Hsuan Liu and Tsung-Hsien Lin National Taiwan University</i></p> <p>TeleProbe: Zero-Power Contactless Probing for Implantable Medical Devices <i>Woo Suk Lee¹, Younghyun Kim² and Vijay Raghunathan³</i> ¹Microsoft, ²University of Wisconsin-Madison, ³Purdue University</p> <p>Retention State-Aware Energy Management for Efficient Nonvolatile Processors <i>Dongqin Zhou¹, Weiwen Chen¹, Xin Shi², Mengying Zhao³ and Keni Qiu¹⁴</i> ¹Capital Normal University, ²Tsinghua University, ³Shandong University, ⁴Beijing Advanced Innovation Center for Imaging Technology</p> <p>1.4-mW, 56-GHz Arithmetic Logic Unit Based on Superconductor Single-Flux-Quantum Logic Circuit <i>Masamitsu Tanaka¹, Ryo Sato¹, Yuki Hatanaka¹, Yuichiro Matsui¹, Hiroyuki Akaike¹, Akira Fujimaki¹, Koki Ishida², Takatsugu Ono² and Koji Inoue²</i> ¹Nagoya University, ²Kyushu University</p> <p>A Reconfigurable Building Block for Thermoelectric Generator Energy Harvesting under Spatial</p>
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	<p>Online Tuning of Dynamic Power Management for Efficient Execution of Interactive Workloads <i>James R. B. Bantock, Vasileios Tenentes, Bashir M. Al-Hashimi and Geoff V. Merrett</i> <i>University of Southampton</i></p> <p>Workload-Driven Frequency-Aware Battery Sizing <i>Yukai Chen, Enrico Macii and Massimo Poncino</i> <i>Politecnico di Torino</i></p> <p>Exploring Sparsity of Firing Activities and Clock Gating for Energy-Efficient Recurrent Spiking Neural Processors <i>Yu Liu, Yingyezhe Jin and Peng Li</i> <i>Texas A&M University</i></p> <p>QuARK: Quality-Configurable Approximate STT-MRAM Cache by Fine-Grained Tuning of Reliability-Energy Knobs <i>Amir Mahdi Hosseini Monazzah¹, Majid Shoushtari², Seyed Ghassem Miremadi¹, Amir M. Rahmani²³ and Nikil Dutt²</i> ¹Sharif University of Technology, ²UC Irvine, ³TU Wien</p> <p>Efficient Thermoelectric Cooling for Mobile Devices <i>Youngmoon Lee, Eugene Kim and Kang G. Shin</i> <i>University of Michigan</i></p> <p>Low Power In-Memory Computing based on Dual-Mode SOT-MRAM <i>Farhana Parveen, Shaahin Angizi, Zhezhi He and Deliang Fan</i> <i>University of Central Florida</i></p>	<p>Temperature Variations <i>Jaemin Kim¹, Naehyuck Chang², Donkyu Baek², Youngil Kim² and Donghwa Shin³</i> ¹Seoul National University, ²KAIST, ³Yeungnam University</p>
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	Session 2A Analog Circuit Design Session Chair: <i>Shreyas Sen</i> <i>(Purdue University)</i> [Locke Hall]	Session 2B HW Support for CNNs Session Chair: <i>Ron Dreslinski</i> <i>(University of Michigan)</i> [Archimedes Hall]
14:30 – 15:45	<p>A 0.13pJ/bit, Referenceless Transceiver with Clock Edge Modulation for a Wired Intra-BAN Communication <i>Jihwan Park, Gi-Moon Hong, Mino Kim, Joo-Hyung Chae and Suhwan Kim</i> <i>Seoul National University</i></p> <p>A 32nm, 0.65-10GHz, 0.9/0.3 ps/σ TX/RX jitter Single Inductor Digital Fractional-n Clock Generator for Reconfigurable Serial I/O <i>William Y. Li, Hyung Seok Kim, Kailash Chandrashekar, Khoa Nguyen, Ashoke Ravi</i> <i>Intel Corp.</i></p> <p>A Tunable Ultra Low Power Inductorless Low Noise Amplifier Exploiting Body Biasing of 28 nm FDSOI Technology <i>Jennifer Zaini¹, Frédéric Hameau², Thierry Taxis¹, Dominique Morche¹, Patrick Audebert¹ and Eric Mercier¹</i> ¹CEA Leti, ²University of Bordeaux</p>	<p>CORAL: Coarse-grained Reconfigurable Architecture for Convolutional Neural Networks <i>Zhe Yuan, Yongpan Liu, Jinshan Yue, Jinyang Li and Huazhong Yang</i> <i>Tsinghua University</i></p> <p>XNOR-POP: A Processing-in-Memory Architecture for Binary Convolutional Neural Networks in Wide-IO2 DRAMs <i>Lei Jiang¹, Minje Kim¹, Wujie Wen² and Danghui Wang³</i> ¹Indiana University Bloomington, ²Florida International University, ³Northwestern Polytechnical University</p> <p>Bit-Width Reduction and Customized Register for Low Cost Convolutional Neural Network Accelerator <i>Kyungrak Choi, Woong Choi, Kyungho Shin and Jongsun Park</i> <i>Korea University</i></p>
15:45 – 16:15	Coffee Break	
16:15 – 17:05	Session 3A Energy Storage & Cyber-Physical Systems Session Chair: <i>Enrico Macii</i> <i>(Politecnico di Torini)</i> [Locke Hall]	Session 3B Design Methodologies for Machine Learning Session Chair: <i>Mikko Lipasti</i> <i>(University of Wisconsin-Madison)</i> [Archimedes Hall]

	<p>Battery Assignment and Scheduling for Drone Delivery Businesses <i>Best Paper Nominee</i> Sangyoung Park, Licong Zhang and Samarjit Chakraborty TU München</p> <p>Reconfigurable Thermoelectric Generators for Vehicle Radiators Energy Harvesting Donkyu Baek¹, Caiwen Ding², Sheng Lin², Donghwa Shin³, Jaemin Kim⁴, Xue Lin⁵, Yanzhi Wang² and Naehyuck Chang¹ ¹KAIST, ²Syracuse University, ³Yeungnam University, ⁴Seoul National University, ⁵Northeastern University</p>	<p>Power Optimizations in MTJ-based Neural Networks through Stochastic Computing Ankit Mondal and Ankur Srivastava University of Maryland</p> <p>A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders Subhendu Roy¹, Yuzhe Ma², Jin Miao¹ and Bei Yu² ¹Cadence Design Systems, ²Chinese University of Hong Kong</p>
17:30 – 20:00	Industrial Reception (for all registered attendees) [Living One, National Taiwan University]	

Tuesday, July 25

7:30 – 9:00	Breakfast	
09:00 – 10:00	Keynote II Peering into the Post Moore's Law World Prof. Todd Austin University of Michigan Chair: Thomas Wenisch (University of Michigan) [Forum Hall]	
10:00 – 10:30	Coffee Break	
10:30 – 11:45	Session 4A Low-Voltage & Energy-Efficient Design	Session 4B Approximate & Learn!

	<p>Session Chair: <i>Naehyuck Chang</i> (KAIST) [Locke Hall]</p>	<p>Session Chair: <i>Hsiang-Yun Cheng</i> (Academia Sinica) [Archimedes Hall]</p>
	<p>Comparative Study and Optimization of Synchronous and Asynchronous Comparators at Near-Threshold Voltages <i>Sung Justin Kim, Doyun Kim and Mingoo Seok</i> Columbia University</p> <p>Full Chip Power Benefits with Negative Capacitance FETs <i>Sandeep K. Samal¹, Sourabh Khandelwal², Asif I. Khan¹, Sayeef Salahuddin³, Chenming Hu³ and Sung Kyu Lim¹</i> ¹Georgia Tech, ²Macquarie University, ³UC Berkeley</p> <p>Design High Bandwidth-Density, Low Latency and Energy Efficient On-Chip Interconnect <i>Yong Wang and Hui Wu</i> University of Rochester</p>	<p>AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing <i>Younghyun Kim¹, Setareh Behroozi¹, Vijay Raghunathan² and Anand Raghunathan²</i> ¹University of Wisconsin-Madison, ²Purdue University</p> <p>Approximate Memory Compression for Energy-Efficiency <i>Ashish Ranjan, Arnab Raha, Vijay Raghunathan and Anand Raghunathan</i> Purdue University</p> <p>SENIN: An Energy-Efficient Sparse Neuromorphic System with On-Chip Learning <i>Myung-Hoon Choi, Seungkyu Choi, Jaehyeong Sim and Lee-Sup Kim</i> KAIST</p>
<p>11:45 – 13:15</p>	<p style="text-align: center;">Lunch [2F Just Italian, Just Sleep]</p>	
<p>13:15 – 14:30</p>	<p style="text-align: center;">Session 5A Architecture & Technology Support for Neural Networks</p> <p style="text-align: center;">Session Chair: <i>Tsung-Te Liu</i> (National Taiwan University) [Locke Hall]</p>	<p style="text-align: center;">Session 5B Power Delivery</p> <p style="text-align: center;">Session Chair: <i>Pradip Bose</i> (IBM T. J. Watson Research Center) [Archimedes Hall]</p>
	<p>Monolithic 3D IC Designs for Low-Power Deep Neural Networks Targeting Speech Recognition <i>Kyungwook Chang¹, Deepak Kadetotad², Yu Cao², Jae-Sun Seo²</i></p>	<p>Placement Mitigation Techniques for Power Grid Electromigration <i>Wei Ye¹, Yibo Lin¹, Xiaoqing Xu¹, Wuxi Li², Yiwei Fu², Yongsheng Sun², Canhui Zhan² and David Z. Pan¹</i></p>

	<p>and Sung Kyu Lim¹ ¹Georgia Tech, ²Arizona State University</p> <p>A Programmable Event-Driven Architecture for Spiking Neural Network Evaluation Arnab Roy¹, Swagath Venkataramani², Neel Gala¹, Sanchari Sen², Kamakoti Veezhinathan¹ and Anand Raghunathan² ¹IIT Madras, ²Purdue University</p> <p>An Energy-Efficient and High-Throughput Bitwise CNN on Sneak-Path-Free Digital ReRAM Crossbar Leibin Ni¹, Zichuan Liu¹, Wenhao Song², J. Joshua Yang², Hao Yu¹, Kenwen Wang³ and Yuangang Wang³ ¹Nanyang Technological University, ²University of Massachusetts Amherst, ³Huawei Technologies</p>	<p>¹UT Austin, ²Hisilicon Technologies</p> <p>Spatial and Temporal Scheduling of Clock Arrival Times for IR Hot-Spot Mitigation, Reformulation of Peak Current Reduction. Bhoopal Gunna, Lakshmi Bhamidipati, Houman Homayoun and Avesta Sasan George Mason University</p> <p>Frequency and Time Domain Analysis of Power Delivery Network for Monolithic 3D ICs Kyungwook Chang¹, Shidhartha Das², Saurabh Sinha², Brian Cline², Greg Yeric² and Sung Kyu Lim¹ ¹Georgia Tech, ²ARM</p>
14:30 – 15:00	Coffee Break	
15:00 – 16:40	<p>Session 6A Multi-Scale Energy-Efficient Designs</p> <p>Session Chair: Yiran Chen (Duke University) [Locke Hall]</p>	<p>Session 6B (Special Session) Interaction of Power Management & Security</p> <p>Session Chair: Saibal Mukhopadhyay (Georgia Tech) TBD [Archimedes Hall]</p>
	<p>ShiftMask: Dynamic OLED Power Shifting Based on Visual Acuity for Interactive Mobile Applications Han-Yi Lin¹, Pi-Cheng Hsiu² and Tei-Wei Kuo^{1,2} ¹National Taiwan University, ²Academia Sinica</p>	<p>Ultra-low Energy Security Circuit Primitives for IoT Platforms Sanu Mathew, Sudhir Satpathy, Vikram Suresh and Ram Krishnamurthy Intel Labs</p>

	<p>Signal Strength-Aware Adaptive Offloading for Energy Efficient Mobile Devices <i>Young Geun Kim and Sung Woo Chung</i> <i>Korea University</i></p> <p>Frequency Governors for Cloud Database OLTP Workloads <i>Rathijit Sen and Alan Halverson</i> <i>Microsoft</i></p> <p>Tiguan: Energy-Aware Collision-Free Control for Large-Scale Connected Vehicles <i>Minghua Shen and Guojie Luo</i> <i>Peking University</i></p>	<p>Low Power Requirements and Side-Channel Protection of Encryption Engines: Challenges and Opportunities <i>Monodeep Kar¹, Arvind Singh¹, Sanu Mathew², Anand Rajan², Vivek De² and Saibal Mukhopadhyay¹</i> ¹Georgia Tech, ²Intel Labs</p> <p>Resilient, Energy-Secure Power Management <i>Pradip Bose and Alper Buyuktosunoglu</i> <i>IBM T. J. Watson Research Center</i></p> <p>Secure Swarm Intelligence: A New Approach to Many-Core Power/Thermal Management <i>Augusto Vega, Alper Buyuktosunoglu and Pradip Bose</i> <i>IBM T. J. Watson Research Center</i></p>
17:30 – 20:30	<p>Banquet [12F Kunlun Hall, The Grand Hotel]</p>	

Wednesday, July 26

7:30 – 9:00	Breakfast
09:00 – 10:00	<p>Keynote III Architecture and Software for Emerging Low-Power Systems <i>Prof. Wen-Mei W. Hwu</i> <i>University of Illinois Urbana-Champaign</i></p> <p>Chair: <i>David Garrett (Broadcom)</i> [Forum Hall]</p>
10:00 – 10:30	Coffee Break

10:30 – 11:45	<p align="center">Session 7A Emerging Technologies</p> <p align="center">Session Chair: <i>David Brooks</i> (<i>Harvard University</i>) [Locke Hall]</p>	<p align="center">Session 7B Low-Power HW Security</p> <p align="center">Session Chair: <i>Sanu Mathew</i> (<i>Intel Labs</i>) [Archimedes Hall]</p>
	<p>Transistor-Level Monolithic 3D Standard Cell Layout Optimization for Full-Chip Static Power Integrity <i>Bon Woong Ku¹, Taigon Song², Arthur Nieuwoudt² and Sung Kyu Lim¹</i> ¹Georgia Tech, ²Synopsys</p> <p>Secure Human-Internet Using Dynamic Human Body Communication <i>Shovan Maity, Debayan Das, Xinyi Jiang and Shreyas Sen</i> <i>Purdue University</i></p> <p>Hotspot Monitoring and Temperature Estimation with Miniature On-Chip Temperature Sensors <i>Pavan Kumar Chundi, Yini Zhou, Martha Kim, Eren Kursun and Mingoo Seok</i> <i>Columbia University</i></p>	<p>A Data Remanence based Approach to Generate 100% Stable Keys from an SRAM Physical Unclonable Function <i>Best Paper Nominee</i> <i>Muqing Liu, Chen Zhou, Qianying Tang, Keshab K. Parhi and Chris H. Kim</i> <i>University of Minnesota</i></p> <p>An Improved Clocking Methodology for Energy Efficient Low Area AES Architectures using Register Renaming <i>Siva Nishok Dhanuskodi and Daniel Holcomb</i> <i>University of Massachusetts Amherst</i></p> <p>A Low-Power APUF-based Environmental Abnormality Detection Framework <i>Hongxiang Gu, Teng Xu and Miodrag Potkonjak</i> <i>UC Los Angeles</i></p>
11:45 – 12:00	Closing Remarks [Forum Hall]	
12:00 – 12:30	Sack Lunch	
12:30 –	<p align="center">Embedded Tutorial Tiny Light-Harvesting Photovoltaic Charger-Supplies <i>Gabriel A. Rincón-Mora</i> <i>Georgia Tech</i> [Forum Hall]</p>	<p align="center">Excursions (Optional, tickets can be purchased at the online registration system)</p>