MONDAY, July 29th, 2019

08:00 – 08:30	**Conference Registration**	
08:30 – 09:00	**Welcome by General and Program Co-Chairs**	
09:00 – 10:00	**Keynote Talk 1: Prof. Giovanni De Micheli, EPFL "Nanosystems: Technology and Tools"**	
10:00 – 10:30	**Coffee Break**	
10:30 – 11:45	**Session 1.1/1.2 .A Low Power Analog Sensing**	**Session 2.1.A Power Delivery: Generate, Regulate, Infiltrate**
12:00 – 13:30	**Lunch**	
13:30 – 14:45	**Session 1.1/1.2 .B Clocking and Communication Techniques**	**Session 2.2.A Low-Power Architectures and Frameworks for Machine Learning**
14:45 – 15:15	**Coffee Break**	
15:15 – 16:30	**Session 1.3.A Low Power On-Chip and Chip-To-Chip Communication**	**Session 2.3.A Artificial Intelligence in System Design**
16:30 – 17:30	**Design Contest Short Presentations**	
17:45 – 19:30	**Industry Reception with Demos and Industry Perspective Posters**	

Session 1.1/1.2.A: Low Power Analog Sensing
Chairs: Frank Gurkaynak, (ETHZ)

10:30 – 10:55 **A Pulse-Width Modulated Cochlear Implant Interface Electronics with 513 µW Power Consumption**
Halil Andac Yigit, Hasan Ulusan, Muhammed Berat Yuksel, Salar Chamanian, Berkay Çiftci, Aziz Koyuncuoglu, Ali Muhtaroglu and Haluk Kulah

10:55 – 11:20 **A Sound Activity Detector Embedded Low-Power MEMS Microphone Readout Interface for Speech Recognition**
Youngtae Yang, Junsoo Cho, byunggyu lee and Suhwan Kim

11:20 – 11:45 **A Compact Self-Capacitance Sensing Analog Front-End for a Touch Detection in Low Power Mode**
Jiheon Park, Young-Ha Hwang, Jonghyun Oh, Yoonho Song, Jun-Eun Park and Deog-Kyoon Jeong

Session 2.1.A: Power Delivery: Generate, Regulate, Infiltrate
Chairs: Mohamed Sabry (NTU)

10:30 – 10:55	**A Design Framework for Thermal-Aware Power Delivery Network in 3D MPSoCs with Integrated Flow Cell Arrays** Halima Najibi, Alexandre Levisse and Marina Zapater
10:55 – 11:20	**Automatic GDSII Generator for On-Chip Voltage Regulator for Easy Integration in Digital SoCs** Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh and Saibal Mukhopadhyay
11:20 – 11:45	**Power Delivery Resonant Virus: Concept and Application** Tianhao Shen, Di Gao, Yiyu Shi and Cheng Zhuo

Session 1.1/1.2.B: Clocking and Communication Techniques
Chairs: Vishal Khatri (IBM)

13:30 – 13:55	**A Low-Energy Inductive Transceiver using Spike-Latency Encoding for Wireless 3D Integration** Benjamin Fletcher, Shidhartha Das and Terrence Mak
13:55 – 14:20	**A Low-Power and Low-Noise 20:1 Serializer with Two Calibration Loops in 55-nm CMOS** Yong-Un Jeong, Joo-Hyung Chae, Sung-Phil Choi, Jaekwang Yun, Shinhyun Jeong and Suhwan Kim
14:20 – 14:45	**Robust Low Power Clock Synchronization for Multi-Die Systems** Ragh Kuttappa, Baris Taskin, Scott Lerner, Vasil Pano and Ioannis Savidis

Session 2.2.A: Low-Power Architectures and Frameworks for Machine Learning
Chairs: Marina Zapater (EPFL), Qing Wu (US Airforce Research)

13:30 – 13:55	**An Automated Approximation Methodology for Arithmetic Circuits** Sayandip De, Jos Huisken and Henk Corporaal
13:55 – 14:20	**An Ultra-Efficient Memristor-Based DNN Framework with Structured Pruning and Quantization Using ADMM** Geng Yuan, Xiaolong Ma, Caiwen Ding, Sheng Lin, Tianyun Zhang, Zeinab S. Jalali, Yilong Zhao, Li Jiang, Sucheta Soundarajan and Yanzhi Wang
14:20 – 14:45	**DYSPINDLE : DYNAMIC SPIKE BUNDLING FOR ENERGY-EFFICIENT SPIKING NEURAL NETWORKS** Sarada Krithivasan, Sanchari Sen, Swagath Venkataramani and Anand Raghunathan

Session 1.3.A: Low Power On-Chip and Chip-To-Chip Communication
Chairs:

15:15 – 15:45	**On Trade-off Between Static and Dynamic Power Consumption in NoC Power Gating** Di Zhu, Yunfan Li and Lizhong Chen
15:45 – 16:10	**Muffin: Minimally-Buffered Zero-Delay Power-Gating Technique in On-Chip Routers** Hossein Farrokhbakht, Hadi Mardani Kamali and Natalie Enright Jerger
16:10 – 16:35	**Concurrent Multipoint-to-Multipoint Communication on Interposer Channels** Lejie Lu, Richard Afoakwa, Michael Huang and Hui Wu

Session 2.3.A: Artificial Intelligence in System Design
Chairs: Amir Aminifar (EPFL)

15:15 – 15:45	**TEA-DNN: the Quest for Time-Energy-Accuracy Co-optimized Deep Neural Networks** Lile Cai, Anne-Maelle Barneche, Arthur Herbout, Chuan Sheng Foo, Jie Lin, Vijay Ramaseshan Chandrasekhar and Mohamed M. Sabry
15:45 – 16:10	**CNN-based Camera-less User Attention Detection for Smartphone Power Management** Daniele Jahier Pagliari, Matteo Ansaldi, Enrico Macii and Massimo Poncino
16:10 – 16:35	**MemGANs: Memory Management for Energy-Efficient Acceleration of Complex Computations in Hardware Architectures for Generative Adversarial Networks** Muhammad Abdullah Hanif, Muhammad Zuhaib Akbar, Rehan Ahmed, Semeen Rehman, Axel Jantsch and Muhammad Shafique

TUESDAY, July 30th, 2019

09:00 – 10:00	**Keynote Talk 2**	
10:00 – 10:30	**Coffee Break**	
10:30 – 11:45	**Session 1.1/1.2 .C Machine Learning Circuits and Memory Design**	**Session 2.2.B Low-Power Edge Computing Systems**
12:00 – 13:30	**Lunch**	
13:30 – 14:45	**Session 1.3.B Approximation for High Energy and Computational Efficiency**	**Session 2.3.B Energy-Efficient Software for Mobile Applications**
14:45 – 15:15	**Coffee Break**	
15:15 – 16:30	**Session 1.3.C Memory Efficiency Improvement**	**Special Session In-Memory Computing**
18:30 –	**Banquet + Awards**	

Session 1.1/1.2.C: Machine Learning Circuits and Memory Design
Chairs: Alexandre Levisse (EPFL)

10:30 – 10:55 **K-Nearest Neighbor Hardware Accelerator Using In-Memory Computing SRAM**
Jyotishman Saikia, Shihui Yin, Zhewei Jiang, Mingoo Seok and Jae-sun Seo

10:55 – 11:20 **A Logic Compatible 4T Dual Embedded DRAM Array for In-Memory Computation of Deep Neural Networks**
Taegeun Yoo, Hyunjoon Kim, Qian Chen, Tony Tae-Hyoung Kim and Bongjin Kim

11:20 – 11:45 **A 65nm switched source line sub-threshold ROM using data encoding, with 0.3V Vmin and 47fJ/b access energy**
Supreet Jeloka, Pranay Prabhat, Graham Knight and James Myers

Session 2.2.B: Low-power Edge Computing Systems
Chairs:

10:30 – 10:55 **Autonomous I/O for Intermittent IoT Systems**
Yu-Chen Lin, Pi-Cheng Hsiu and Tei-Wei Kuo

10:55 – 11:20 **BottleNet: A Deep Learning Architecture for Intelligent Mobile Cloud Computing Services**
Amir Erfan Eshratifar, Amirhossein Esmaili and Massoud Pedram

11:20 – 11:45 **Similarity-Based LSTM Architecture for Energy-Efficient Edge-Level Speech Recognition**
Junseo Joe, Jaeha Kung, Sunggu Lee and Youngjoo Lee

Session 1.3.B: Approximation for High Energy and Computational Efficiency
Chairs:

13:30 – 13:55 **MixNet: An Energy-Scalable and Computationally Lightweight Deep Learning Accelerator**
Sangwoo Jung, Seungsik Moon, Youngjoo Lee and Jaeha Kung

13:55 – 14:20 **A^2M: Approximate Algebraic Memory Using Polynomial Rings**
Dong Kai Wang and Nam Sung Kim

14:20 – 14:45 **Compressing Sparse Ternary Weight Convolutional Neural Networks for Efficient Hardware Acceleration**
Hyeonwook Wi, Hyeonuk Kim, Seungkyu Choi and Lee-sup Kim

Session 2.3.B: Energy-Efficient Software for Mobile Applications
Chairs:

13:30 – 13:55 **FLASH: Content-based Power-saving Design for Scrolling Operations in Browser Applications on Mobile OLED Devices**
Hao-Chun Chang, Yu-Chieh Yang, Liang-Yan Yu and Chun-Han Lin

13:55 – 14:20 **Balancing Memory Accesses for Energy-Efficient Graph Analytics Accelerators**
Mingyu Yan, Xing Hu, Shuangchen Li, Itir Akgun, Han Li, Xin Ma, Lei Deng, Xiaochun Ye, Zhimin Zhang, Dongrui Fan and Yuan Xie

14:20 – 14:45 **Rethinking Last-level-cache Write-back Strategy for MLC STT-RAM Main Memory with Asymmetric Write Energy**
Yu-Pei Liang, Tseng-Yi Chen, Yuan-Hao Chang, Shuo-Han Chen, Pei-Yu Chen and Wei-Kuan Shih

Session 1.3.C: Memory Efficiency Improvement
Chairs:

15:15 – 15:45 **Improving Energy Efficiency by Memorizing Data Access Information**
Michael Stokes, Ryan Baird, Zhaoxiang Jin, David Whalley and Soner Onder

15:45 – 16:10 **Exploring the Relation between Monolithic 3D L1 GPU Cache Capacity and Warp Scheduling Efficiency**
Cong Thuan Do, Young-Ho Gong, Cheol Hong Kim, Seon Wook Kim and Sung Woo Chung

16:10 – 16:35 **SHRIMP: Efficient Instruction Delivery with Domain Wall Memory**
Joonas Multanen, Asif Ali Khan, Pekka Jääskeläinen, Fazal Hameed and Jeronimo Castrillon

Special Session: In-Memory Computing
Chairs:

15:15 – 15:45 TBD

15:45 – 16:10 TBD

16:10 – 16:35 TBD

WEDNESDAY July 31st, 2019

09:00 – 10:00	**Keynote Talk 3**	
10:00 – 11:00	**Poster Session with Coffee Break**	
11:00 – 12:15	**Session 1.3/2.3.D Application-Centric Optimization of Emerging Technologies**	**Session 2.1/2.2/2.3 TBD**
12:15 – 12:30	**Closing Remarks**	
12:30 – 14:00	**Lunch**	

Session 1.3/2.3.D: Application-Centric Optimization of Emerging Technologies
Chairs:

10:30 – 10:55 **RAPID: A ReRAM Processing in Memory Architecture for DNA Sequence Alignment**
Saransh Gupta, Mohsen Imani, Behnam Khaleghi, Venkatesh Kumar and Tajana Rosing

10:55 – 11:20 **HR3AM: a Heat Resilient design for RRAM based neuromorphic computing**
Xiao Liu, Minxuan Zhou, Tajana Rosing and JISHEN ZHAO

11:20 – 11:45 **NCFET-Aware Voltage Scaling**
Sami Salamin, Martin Rapp, Hussam Amrouch, Girish Pahwa, Yogesh Chauhan and Joerg Henkel

Session 2.1/2.2/2.3: TBD
Chairs:

10:30 – 10:55 **Towards a Complete Methodology for Synthesizing Bundled-Data Asynchronous Circuits on FPGAs**
Kshitij Bhardwaj, Paolo Mantovani, Luca Carloni and Steven M. Nowick

10:55 – 11:20 **Tier Partitioning and Flip-flop Relocation Methods for Clock Trees in Monolithic 3D ICs**
Da Eun Shim, Sai Surya Kiran Pentapati, Jeehyun Lee and Sung Kyu Lim

11:20 – 11:45 **VCAM: Variation Compensation through Activation Matching for Analog Binarized Neural Networks**
Jaehyun Kim, Chaeun Lee, Jihun Kim, Yumin Kim, Cheol Seong Hwang and Kiyoung Choi

Poster Session
Chairs:

1 **3DTUBE: A DESIGN FRAMEWORK FOR HIGH-VARIATION CARBON NANOTUBE-BASED TRANSISTOR TECHNOLOGY**
Aporva Amarnath, Javad Bagherzadeh, Jielun Tan and Ron Dreslinski

2 **A PROBABILISTIC APPROACH TO ENERGY-CONSTRAINED MIXED-CRITICALITY SYSTEMS**
Federico Reghenzani, Giuseppe Massari and William Fornaciari

3 **ADDRESSING TEMPORAL VARIATIONS IN QUBIT QUALITY METRICS FOR PARAMETERIZED QUANTUM CIRCUITS**
MAHABUBUL ALAM, Abdullah Ash- Saki and Swaroop Ghosh

4 **AN ENERGY EFFICIENT ON-CHIP LEARNING ARCHITECTURE FOR STDP BASED SPARSE CODING**
Heetak Kim, Hoyoung Tang and Jongsun Park

5 **BATTERY-AWARE ELECTRIC TRUCK DELIVERY ROUTE PLANNER**

	Donkyu Baek, Yukai Chen, Naehyuck Chang, Enrico Macii and Massimo Poncino
6	**COMPHD: EFFICIENT HYPERDIMENSIONAL COMPUTING USING MODEL COMPRESSION** Justin Morris, Mohsen Imani, Samuel Bosch, Anthony Thomas, Helen Shu and Tajana Rosing
7	**FPGA-based Acceleration of Binary Neural Network Training with Minimized Off-Chip Memory Access** Pavan Kumar Chundi, Peiye Liu, Sangsu Park, Seho Lee and Mingoo Seok
8	**ENERGY-AUTONOMOUS MCU OPERATING IN SUB-VT REGIME WITH TIGHTLY-INTEGRATED ENERGY-HARVESTER** Jian Deng, Jean-Luc Nagel, Loïc Zahnd, Marc Pons, David Ruffieux, Claude Arm, Pascal Persechini and Stephane Emery
9	**LOCAL LEARNING IN RRAM NEURAL NETWORKS WITH SPARSE DIRECT FEEDBACK ALIGNMENT** Brian Crafton, Pradip Basnet, Matthew West, Eric Vogel and Arijit Raychowdhury
10	**MESSAGEFUSION: ON-PATH MESSAGE COALESCING FOR ENERGY EFFICIENT AND SCALABLE GRAPH ANALYTICS** Leul Belayneh, Abraham Addisie and Valeria Bertacco
11	**MODELING AND OPTIMIZATION OF CHIP COOLING WITH TWO-PHASE VAPOR CHAMBERS** Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Sherief Reda, Evelyn Wang and Ayse Coskun
12	**NON-VOLATILE MEMORY UTILIZING RECONFIGURABLE FERROELECTRIC TRANSISTORS TO ENABLE DIFFERENTIAL READ AND ENERGY-EFFICIENT IN-MEMORY COMPUTATION.** Sandeep Krishna Thirumala, Shubham Jain, Anand Raghunathan and Sumeet Gupta
13	**SECO: A SCALABLE ACCURACY APPROXIMATE EXPONENTIAL FUNCTION VIA CROSS-LAYER OPTIMIZATION** Di Wu, Tianen Chen, Chien-fu Chen, Oghenefego Ahia, Joshua San Miguel, Mikko Lipasti and Younghyun Kim
14	**SHINE: A NOVEL SHA-3 IMPLEMENTATION USING RERAM-BASED IN-MEMORY COMPUTING** Karthikeyan Nagarajan, Sina Sayyah Ensan, Mohammad Nasim Imtiaz Khan, Swaroop Ghosh and Anupam Chattopadhyay
15	**TEMPERATURE-AWARE ADAPTIVE VM ALLOCATION IN HETEROGENEOUS DATA CENTERS** Young Geun Kim, Jeong In Kim, Seung Hun Choi, Seon Young Kim and Sung Woo Chung
16	**TIP: A TEMPERATURE EFFECT INVERSION-AWARE ULTRA-LOW POWER SYSTEM-ON-CHIP PLATFORM** Kyuseung Han, Sukho Lee, Jae-Jin Lee, Woojoo Lee and Massoud Pedram