ISLPED 2023

INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

AUGUST 7–8, 2023, TU WIEN, VIENNA, AUSTRIA

Updated on August 4
Welcome Reception and Conference (Sunday to Tuesday)
Institut für Computertechnik der TU Wien
Address: Gußhausstr. 27-29, 1040 Vienna
Welcome Reception (Sun) @ Rooftop (6th floor)
Conference (Mon/Tue) @ Ground floor
Banquet Dinner (Monday)
Fuhrgassl-Huber, Weingut und Buschenschank
Address: Neustift am Walde 68, 1190 Vienna

Public Transportation Guide

Overall route from the conference site to the restaurant.

1. Take Metro Line **U4** at **Karlsplatz** station (600 m, 7 min walk).

2. Get off at **Spittelau** station (10 min, 7 stops). Take Bus Line **35A** at **Spittelau S+U** station (400 m, 5 min walk).

3. Get off at **Neustift am Walde** station (21 min, 16 stops). The restaurant is 1 min walk ahead.
PROGRAM OVERVIEW

Sunday, August 6
18:00–22:00 Welcome Reception (6th floor rooftop)

Monday, August 7
7:30–8:00 Registration
8:00–8:30 Welcome
8:30–9:30 Keynote 1
Radu Marculescu
"Thirty Years of Low-Power Design: From Watts to Wisdom"
9:30–9:45 Coffee Break
9:45–10:45 Special Session
Aida Todri-Sanial, Sudeep Pasricha, and Partha Pande (Organizer)
"Energy-Efficient ML Acceleration: From Technologies to Circuits and Systems"
10:45–11:00 Coffee Break
11:00–12:20 Session 1A
“Energy-Efficient Memory and Processing”
Session 1B
“Performance- and Energy-Aware Acceleration and Tensor Processing”
12:20–14:00 Lunch (Main Hall) & Poster Session (Side Hall)
14:00–15:00 Design Contest
15:00–15:10 Coffee Break
15:10–16:30 Session 2A
“Energy-Efficient Sensors, Processors, and Middleware”
Session 2B
“Energy-Efficient Hardware Acceleration of GNN and Transformers”
16:30–19:30 Break
19:30– Banquet Dinner
Buschenschank Fuhrgassl-Huber

Tuesday, August 8
7:30–8:00 Registration
8:00–9:00 Keynote 2
Jan Rabaey
"Lessons from the Brain"
9:00–9:10 Coffee Break
9:10–10:40 Panel Discussion
Massoud Pedram (Organizer), Ajay Joshi (Moderator), Ahmed Hemani, Axel Jantsch, Diana Marculescu, Radu Marculescu, and Aida Todri-Sanial
"Artificial General Intelligence: A Technological Marvel or an Existential Question"
10:40–10:50 Coffee Break
10:50–12:10 Session 3A
“ML-Driven Automation and Multi-Objective Optimization for Low-Power Design”
Session 3B
“Novel Processing-in-Memory Techniques for Low Power”
12:10–13:50 Lunch (Main Hall) & Poster Session (Side Hall)
13:50–15:10 Session 4A
“When Low Power Design Meets Hardware Security”
Session 4B
“Low Power AI Accelerators and AI for Low Power Design”
15:10–15:20 Coffee Break
15:20–16:20 Session 5A
“Novel Parallel Architectures for Deep Learning”
16:20–16:30 Closing Remarks and Awards
MONDAY PROGRAM

8:30–9:30  
EI8 Pötzl  
**Keynote 1**  
Chair: Umit Ogras, University of Wisconsin–Madison  
*Thirty Years of Low-Power Design: From Watts to Wisdom*  
Radu Marculescu, University of Texas at Austin

9:45–10:45  
**Special Session**  
Organizer: Partha Pande, Washington State University  
*Energy-Efficient ML Acceleration: From Technologies to Circuits and Systems*  
Aida Todri-Sanial, Eindhoven University of Technology  
Sudeep Pasricha, Colorado State University  
Partha Pande (Organizer), Washington State University

11:00–12:20  
EI8 Pötzl  
**Session 1A: “Energy-Efficient Memory and Processing”**  
Chair: Alexander Fish, Bar-Ilan University

- 11:00–11:20  
  A Comparative Study on Front-Side, Buried and Back-Side Power Rail topologies in 3nm technology node  
  Sandra Shaji, Lingjun Zhu, Junsik Yoon and Sung Kyu Lim

- 11:20–11:40  
  CoolDRAM: An Energy-Efficient and Robust DRAM *(Best Paper Candidate)*  
  Nezam Rohbani, Mohammad Arman Soleimani and Hamid Sarbazi-Azad

- 11:40–12:00  
  Development of Tropical Algebraic Accelerator with Energy Efficient Time-Domain Computing for Combinatorial Optimization and Machine Learning  
  Qiankai Cao, Xi Chen and Jie Gu

- 12:00–12:20  
  IMBUE: In-Memory Boolean-to-Current Inference Architecture for Tsetlin Machines  
  Omar Ghazal, Simranjeet Singh, Tousif Rahman, Shengqi Yu, Yujin Zheng, Domenico Balsamo, Sachin Patkar, Farhad Merchant, Fei Xia, Alex Yakovlev and Rishad Shaﬁk

11:00–12:20  
EI9 Hlawka  
**Session 1B: “Performance- and Energy-Aware Acceleration and Tensor Processing”**  
Chair: Ganapati Bhat, Washington State University

- 11:00–11:20  
  iMAT: Energy-Efficient In-Memory Acceleration of Ternary Neural Networks With Sparse Dot Product *(Best Paper Candidate)*  
  Shien Zhu, Shuo Huai, Guochu Xiong and Weichen Liu

- 11:20–11:40  
  Accelerating ML-adjacent Computation Using Tensor Processors  
  Dongho Ha, Won Woo Ro and Hung-Wei Tseng

- 11:40–12:00  
  Energy-Harvesting-Aware Adaptive Inference of Deep Neural Networks in Embedded Systems  
  Gwanjong Park, Osama Khan and Euiseong Seo

- 12:00–12:20  
  Precision-aware Latency and Energy Balancing on Multi-Accelerator Platforms for DNN Inference  
  Matteo Risso, Alessio Burrello, Giuseppe Maria Sarda, Luca Benini, Enrico Macii, Massimo Poncino, Marian Verhelst and Daniele Jahier Pagliari

12:20–14:00  
**Lunch & Poster Session**  
List of posters on p. 9

14:00–15:00  
EI8 Pötzl  
**Design Contest**  
Co-Chairs: Rajesh Kedia, IIT Hyderabad; Florian Huemer, TU Wien

- 14:00–14:03  
  Energy Aware Time Series Classification for Low-Power Microcontrollers  
  Matthias Bittner, Dominik Dallinger, Matthias Wess, Daniel Schnoell, and Axel Jantsch
14:03–14:06  **A Low-Power RISC-V Multicore Processor with a Shared Lightweight FPU**  
Jina Park, Eunjin Choi, Woojoo Lee, Sukho Lee, Jae-Jin Lee, and Massoud Pedram

14:06–14:09  **SmartHeaP - A High-level Programmable, Low Power, and Mixed-Signal Hearing Aid SoC in 22nm FD-SOI**  
Jens Karrenbauer, Simon Klein, Sven Schönewald, Lukas Gerlach, Meinolf Blawat, Jens Benndorf and Holger Blume

14:09–14:12  **Object Detection on a Nano-Drone Using a RISC-V Multi-Core MCU Accelerator**  
Luca Bompani, Lorenzo Lamberti, Victor Javier Kartsch, Manuele Rusci, Daniele Palossi and Luca Benini

14:12–14:15  **PLP-DVS: Adaptive Energy Scaling of Capacitor-Based Power Loss Protection in SSDs**  
Jaehyuck Cho, Jeongmin Jeongmin Choi, Sunghyun Park, Jiyoung Kim, Sungjun Yun, Kyungmin Lim, Jaehyun Park, Sungyong Ahn, and Donghwa Shin

14:15–14:18  **A Passive Bidirectional BLE Tag Demonstrating Battery-Free Communication in Tablet/Smartphone-to-Tag, Tag-to-Tablet/Smartphone, and Tag-to-Tag Modes**  
Ziyi Chang, Qijing Xiao, Cheng Chen, Yuxuan Luo, and Bo Zhao

14:18–14:21  **TunnelTx: Demonstrating Low-Power Wireless Transmissions using Tunnel Diode based Wireless Transmitters**  
Wenqing Yan, Manoj Gulati, Prabal Dutta, and Ambuj Varshney

14:21–15:00  Live demo and poster presentation

15:10–16:30  **Session 2A: “Energy-Efficient Sensors, Processors, and Middleware”**  
Chair: Jaehyun Park, University of Ulsan

15:10–15:30  **Florian: Developing a Low-power RISC-V Multicore Processor with a Shared Lightweight FPU**  
Jina Park, Kyuseung Han, Eunjin Choi, Sukho Lee, Jae-Jin Lee, Woojoo Lee and Massoud Pedram

15:30–15:50  **Energy Efficient Real-Time Scheduling on Heterogeneous Architectures with Self-Suspension Model**  
Wenwen Xu, Zheyu Zhang, Yuankai Xu, Jing Li, Yehan Ma, Yier Jin, Chris Gill, Xuan Zhang and An Zou

15:50–16:10  **CARMA: Context-Aware Runtime Reconfiguration for Energy-Efficient Sensor Fusion**  
Yifan Zhang, Arnav Malawade, Xiaofang Zhang, Yuhui Li, DongHwan Seong, Mohammad Al Faruque and Sitao Huang

16:10–16:30  **Uncertainty-aware Online Learning for Dynamic Power Management in Large Manycore systems**  
Gaurav Narang, Raid Ayoub, Michael Kishinevsky, Jana Doppa and Partha Pratim Pande

15:10–16:30  **Session 2B: “Energy-Efficient Hardware Acceleration of GNN and Transformers”**  
Chair: Nee Arman Roohi, University of Nebraska

15:10–15:30  **A Multicore GNN Training Accelerator**  
Sudipta Mondal, Ramprasath S, Ziqing Zeng, Kishor Kunal and Sachin S. Sapatnekar

15:30–15:50  **Joint Optimization of Cache Management and Graph Reordering for GCN Acceleration**  
Kyeong-Jun Lee, ByungJun Kim, Han-Gyeol Mun, Seunghyun Moon and Jae-Yoon Sim

15:50–16:10  **ITA: An Energy-Efficient Attention and Softmax Accelerator for Quantized Transformers**  
Gamze Islamoglu, Moritz Scherer, Gianna Paulin, Tim Fischer, Victor Jung, Angelo Garofalo and Luca Benini

16:10–16:30  **Energy-Efficient RISC-V-Based Vector Processor for Cache-Aware Structurally-Pruned Transformers**  
Jung Gyu Min, Dongyoun Kam, Younghoon Byun, Gunho Park and Youngjoo Lee
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<td>Keynote 2</td>
<td>Lessons from the Brain&lt;br&gt;Jan M. Rabaey, University of California, Berkeley</td>
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<td>9:10–10:40</td>
<td>Panel Discussion</td>
<td>Artificial General Intelligence: A Technological Marvel or an Existential Question&lt;br&gt;Massoud Pedram (Organizer), University of Southern California; Ajay Joshi, Boston University and Lightmatter; Ahmed Hemani, KTH Royal Institute of Technology; Axel Jantsch, Technische Universität Wien; Diana Marculescu, University of Texas at Austin; Radu Marculescu, University of Texas at Austin; Aida Todri-Sanial, Technische Universiteit Eindhoven</td>
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<td>10:50–12:10</td>
<td>Session 3A: “ML-Driven Automation and Multi-Objective Optimization for Low-Power Design”</td>
<td>Machine Learning Driven Synthesis of Clock Gating&lt;br&gt;Doyeon Won, Soomin Kim and Taewhan Kim&lt;br&gt;Automatic Generation of Cell Based Structured CIM Macros&lt;br&gt;Christian Lanius, Jie Lou, Johnson Loh and Tobias Gemmeke&lt;br&gt;Multi-objective optimization for Floating Point Mix-Precision Tuning (Best Paper Candidate)&lt;br&gt;Zeqing Li and Youhui Zhang&lt;br&gt;REFROM: Responsive, Energy-efficient Frame Rendering for Mobile Devices (Best Paper Candidate)&lt;br&gt;Tsung-Yen Hsu, Yi-Shen Chen, Yun-Chih Chen, Yuan-Hao Chang and Tei-Wei Kuo</td>
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<td>12:10–13:50</td>
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13:50–14:10  **Low Power Logic Obfuscation Through System Level Clock Gating**  
Daniel Xing, Yuntao Liu and Ankur Srivastava

14:10–14:30  **FPGA-Patch: Mitigating Side Channel Attacks on Multi-Tenant FPGAs using Dynamic Patch Generation (Best Paper Candidate)**  
Mahya Morid Ahmadi, Lilas Alrahis, Ozgur Sinanoglu and Muhammad Shafique

14:30–14:50  **Enabling DVFS Side-Channel Attacks for Neural Network Fingerprinting in Edge Inference Services**  
Erich Malan, Valentino Peluso, Andrea Calimera and Enrico Macii

14:50–15:10  **Hardware Trojans in fdSOI**  
Christian Lanius, Florian Freye, Shutao Zhang and Tobias Gemmeke

13:50–15:10  **Session 4B: “Low Power AI Accelerators and AI for Low Power Design”**  
Chair: Younghyun Kim, University of Wisconsin–Madison

13:50–14:10  **Bridging the Gap between Spiking Neural Networks & LSTMs for Latency & Energy Efficiency**  
Gourav Datta, Haoqin Deng, Robert Aviles, Zeyu Liu and Peter Beerel

14:10–14:30  **Partial-sum Quantization for near ADC-Less Compute-In-Memory Accelerators**  
Utkarsh Saxena and Kaushik Roy

14:30–14:50  **Efficient Multi-Objective Optimization for PVT Variation-Aware Circuit Sizing using Surrogate Models and Smart Corner Sampling**  
Octavian Pascu, Catalin Visan, Georgian Nicolae, Mihai Boldeanu, Horia Cucu, Cristian V. Diaconu, Andi Buzo and Georg Peiz

14:50–15:10  **Model-Driven Dataset Generation for Data-Driven Battery SOH Models**  
Khaled Sidahmed Sidahmed Alamin, Francesco Daghero, Giovanni Pollo, Daniele Jahier Pagliari, Yukai Chen, Enrico Macii, Massimo Poncino and Sara Vinco

15:20–16:20  **Session 5A: “Novel Parallel Architectures for Deep Learning”**  
Chair: Jiang Hu, Texas A&M University

15:20–15:40  **Ocellus: Highly Parallel Convolution-in-Pixel Scheme Realizing Power-Delay-Efficient Edge Intelligence (Best Paper Candidate)**  
Sepehr Tabrizchi, Shaahin Angizi and Arman Roohi

15:40–16:00  **Sky-NN: Enabling Efficient Neural Network Data Processing with Skyrmion Racetrack Memory**  
Yong-Cheng Liao, Shuo-Han Chen, Yuan-Hao Chang and Yu-Pei Liang

16:00–16:20  **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit**  
Hyun Woo Oh, Seongmo An, Won Sik Jeong and Seung Eun Lee
1. Scaled Population Division for Approximate Computing
   Kunal Bharathi, Sunil Khatri and Jiang Hu

2. Cryogenic CMOS as an Enabler for Low Power Dynamic Logic
   Rakshith Saligram, Suman Datta and Arijit Raychowdhury

3. Quantifying the Overheads of Modular Multiplication
   Deepraj Soni, Mohammed Nabeel Thari Moopan, Negar Neda, Ramesh Karri, Michail Maniatakos and Brandon Reagen

4. Multi-Source Transfer Learning for Design Technology Co-Optimization
   Jakang Lee, Jaeseung Lee, Seonghyeon Park and Seokhyeong Kang

5. Enabling Highly-Efficient DNA Sequence Mapping via ReRAM-based TCAM
   Yu-Shao Lai, Shuo-Han Chen and Yuan-Hao Chang

6. A Self-powered Predictive Maintenance System Based on Piezoelectric Energy Harvesting and TinyML
   Zijie Chen, Yiming Gao and Junrui Liang

7. Temperature-Aware Memory Mapping and Active Cooling of Neural Processing Units
   Vahidreza Moghaddas, Hammam Kattan, Tim Buecher, Mikail Yayla, Jian-Jia Chen and Hussam Amrouc

8. WeNet: Configurable Neural Network with Dynamic Weight-Enabling for Efficient Inference
   Jingxiao Ma and Sherief Reda

   Dina Husseini, Taha Belkhouja, Ganapati Bhat and Jana Doppa

    Heewoo Kim, Haojie Ye, Trevor Mudge, Ronald Dreslinski and Nishil Talati

11. Weight-Aware Activation Mapping for Energy-Efficient Convolution on PIM Arrays
    Kang Eun Jeon, Johnny Rhe, Hyeonsu Bang and Jong Hwan Ko

12. Teleport: A High-Performance ShiftNet Hardware Accelerator with Fused Layer Computation
    Hyunmin Kim and Sungji Ryu

13. Energy-Efficient ReRAM-based ML Training via Mixed Pruning and Reconfigurable ADC
    Chukwufumnanya Ogbugo, Biresh Kumar Joardar, Soumen Mohapatra, Jana Doppa, Deukhyoun Heo, Krishnendu Chakrabarty and Partha Pratim Pande

14. Digital Implementation of On-Chip Hebbian Learning for Oscillatory Neural Networks
    Edgar Leonard Marvin Luhulima, Madeleine Abernot, Federico Corradi and Aida Todri-Sanial

15. PAIRS: Pruning-Aided Row-Skipping for SDK-Based Convolutional Weight Mapping in Processing-In-Memory Architectures
    Johnny Rhe, Kang Eun Jeon and Jong Hwan Ko

    Zexi Ji, Hanrui Wang, Miaorong Wang, Win-San Khwa, Meng-Fan Chang, Song Han and Anantha P. Chandrakasan

17. Learning from Output Transitions: A Chosen Challenge Strategy for ML Attacks on PUFs
    Chia-Chih Lin and Ming-Syan Chen

18. Efficient Machine Learning on Encrypted Data using Hyperdimensional Computing
    Yujin Nam, Minxuan Zhou, Saransh Gupta, Gabrielle De Micheli, Rosario Cammarota, Chris Wilkerson, Daniele Micciancio and Tajana Rosing
**General Co-Chairs**  
Swaroop Ghosh, Pennsylvania State University  
Axel Jantsch, Technische Universität Wien

**Technical Program Co-Chairs**  
Umit Ogras, University of Wisconsin–Madison  
Pascal A. Meinerzhagen, Intel Corporation

**Treasurer**  
Mehdi Kamal, University of Southern California

**Local Arrangements Chair**  
Thilo Sauter, Technische Universität Wien  
Maximilian Götzinger, Technische Universität Wien

**Web Chair**  
Meron Zerihun Demissie, University of Michigan

**Publications Chair**  
Younghyun Kim, University of Wisconsin–Madison

**Design Contest Co-Chairs**  
Rajesh Kedia, Indian Institute of Technology Hyderabad  
Florian Huemer, Technische Universität Wien

**Publicity Chair**  
Semeen Rehman, Technische Universität Wien  
Linghao Song, University of California, Los Angeles  
Jae-Joon Kim, Seoul National University
Track 2. CAD, Systems, and Software

2.1. CAD Tools and Methodologies
Enrico Macii (Track Co-Chair), Politecnico di Torino
Azadeh Davoodi (Track Co-Chair), University of Wisconsin-Madison
Alberto Macii, Politecnico di Torino
Pascal Vivet, CEA-Leti
Matthew Ziegler, IBM
Alessio Burrello, University of Bologna
Francesco Regazzoni, USA
Donkyu Baek, Chungbuk National University
Nadine Azemard-Crestani, LIRMM
Sanghamitra Roy, Utah State University

2.2. Systems and Platforms
Marina Zapater (Track Co-Chair), University of Applied Sciences Western Switzerland
Hun Seok Kim (Track Co-Chair), University of Michigan
Donghwa Shin, Soongsil University
Massimo Poncino, Politecnico di Torino
Pai Chou, National Cheng Kung University, Taiwan
Jaehyun Park, University of Ulsan
Mohammad Al Faruque, UC Irvine
Masanori Hashimoto, Osaka University
Hussam Armrouch, University of Stuttgart
Taeyong Kim, Intel
Jason Xue, City University of Hong Kong
William Fornaciari, Politecnico di Melano
Ganapati Bhat, Washington State University

2.3. Software and Applications
Yuan-Hao Chang (Track Co-Chair), Academia Sinica
Xue Lin (Track Co-Chair), North Eastern University
Ittetsu Taniguchi, Osaka University
Wanli Chang, University of York
Daniele Jahier Pagliari, Politecnico di Torino
Young Geun Kim, Korea University
Aporva Amarnath, IBM
Jalil Boukhobza, ENSTA-Bretagne

Track 3. AI/ML Hardware and System Security

3.1. AI/ML Hardware
Aida Todri-Sanial (Track Co-Chair), CNRS-LIRMM/University of Montpellier
Priyadarshini Panda (Track Co-Chair), Yale
Jan Moritz Joseph, RWTH
Amit Trivedi, University of Illinois
Georgios Karakostantis, Queen's University Belfast
Arman Roohi, University of Nebraska
Kanad Basu, University of Texas Dallas
Gokul Krishnan, Arizona State University
Prabal Basu, Cadence
Abhronil Sengupta, Pennsylvania State University
Shaahin Angizi, New Jersey Institute of Technology
Youngjoo Lee, POSTECH
Jason Eshraghian, University of California Santa Cruz
Ivan Miro-Panades, CEA
Srivatsa Rangachar Srinivasa, Intel
Nikita Mirchandani, On Semi
Jae-sun Seo, Arizona State University
Greg Chen, Intel
Phil Knag, IBM
Cedric Lichtenau, IBM
Sumit Mandal, Indian Institute of Science
Jae-Yoon Sim, POSTECH

3.2. Hardware and System Security
Qinru Qiu (Track Co-Chair), Syracuse University
Anupam Chattopadhyay (Track Co-Chair), Nanyang Technological University
Kaveh Shamsi, University of Texas Dallas
Wei Jiang, UESTC
Asmit De, SiFive
Sara Tehranipoor, West Virginia University
Debjyoti Bhattacharjee, IMEC
Debayan Das, Intel
Shivam Bhasin, Nanyang Technological University
Sohrab Aftabjahani, Intel
Jeyavijayan Rajendran, Texas A&M University