INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

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Hilton Waterfront Beach Resort
Huntington Beach, California

FINAL PROGRAM

SUNDAY, August 5, 2001

18:30-20:30 Registration and Welcome Reception

MONDAY, August 6, 2001

7:45-8:45 Continental Breakfast

8:45-9:00 Welcome ***Waterfront Ballroom A-B-C***
Session Chair: Enrico Macii, Politecnico di Torino, General Chair

Symposium Highlights
Mary Jane Irwin, Penn State Univ., Co-TPC Chair

9:00-9:45 Keynote Talk ***Waterfront Ballroom A-B-C***
Session Chair: Vivek De, Intel, Co-TPC Chair

Wireless Beyond the Third Generation: Facing the Energy Challenge
Jan Rabaey, UC Berkeley

9:45-10:00 Coffee Break

9:45-18:00 Exhibits ***Waterfront Ballroom D-E***

10:00-11:30 Session 1: ***Waterfront Ballroom A-B***
Energy Reduction in Processor Pipelines
Session Chair: Pradip Bose, IBM
Session Organizer: Stephen Kosonocky, IBM

1.1 *Micro-Operation Cache: A Power Aware Frontend for Variable Instruction Length ISA*
Baruch Solomon, Avi Mendelson, Doron Orenstien, Yoav Almog, Ronny Ronen, Intel Israel

1.2 *L1 Data Cache Decomposition for Energy Efficiency*
Michael Huang, Jose Renau, Seung-Moon Yoo, Josep Torrellas, UIUC

1.3s *Instruction Flow-Based Frontend Throttling for Power Aware High Performance Processors*
Amirali Baniasadi, Northwestern Univ., Andreas Moshovos, Univ. of Toronto

1.4s *Energy Reduction in Queues and Stacks by Adaptive Bitwidth Compression*
Vasily Moshnyaga, Fukuoka Univ.

10:00-11:30 Session 2: ***Waterfront Ballroom C***
Voltage and Instruction Scheduling
Session Chair: Massoud Pedram, USC
Session Organizer: Luca Benini, Univ. di Bologna

2.1 *Energy Priority Scheduling for Variable Voltage Professors*
Johan Pouwelse, Koen Langendoen, Henk Sips, Delft Univ.

2.2 *Dynamic Voltage Scheduling Techniques for Low Power Multimedia Applications using Buffers*
Chaeseok Im, Huiseok Kim, Soonhoi Ha, Seoul National Univ.

2.3s *Power Aware Modulo Scheduling for High Performance VLIW Processors*
Han-Saem Yun, Jihong Kim, Seoul National Univ.

2.4s *Hard Real-Time Scheduling for Low Energy using Stochastic Data and DVS Processor*
Flavius Gruian, Lund Univ.

11:40-12:15 Poster Session 1 ***Waterfront Ballroom A-B***
Session Chair: Mircea Stan, Univ. of Virginia

P1.1 *Analysis and Design of Low Energy FFs*
Dejan Markovic, Borivoje Nikolic, Robert Brodersen, UCB

P1.2 *Analysis of Clocked Timing Elements for DVS Effects over Process Parameter Variations*
Hoang Dao, UC Davis, Kevin Nowka, IBM Austin, Vojin Oklobdzija, UC Davis

P1.3 *A Low Power Motion Estimation Block for Low Bit-Rate Wireless Video*
Steven Richmond, Hewlett Packard, Dong Ha, Virginia Tech

P1.4 *Power Aware Partitioned Cache Architectures*
Soontae Kim, N. Vijaykrishnan, Mahmut Kandemir, Anand Sivasubramaniam, M.J. Irwin, E. Geethanjali, Penn State Univ.

P1.5 *A Low Leakage Dynamic Multi-Ported Register File in 0.13um CMOS*
Atila Alvandpour, Ram Krishnamurthy, K. Soumyanath, Shekhar Borkar, Intel

P1.6 *Energy Efficient Load and Store Reuse*
Jun Yang, Rajiv Gupta, Univ. of Arizona

11:40-12:15 Poster Session 2 ***Waterfront Ballroom C***
Session Chair: Jorg Henkel, NEC

P2.1 *Compiler Support for Block Buffering*
Mahmut Kandemir, Penn State Univ., J. Ramanujam, LSU, Uger Sezer, Univ. Wisconsin

P2.2 Automatic Source Code Specialization for Energy Reduction
Eui-Young Chung, Stanford, Luca Benini, Univ. di Bologna
Giovanni De Micheli, Stanford

P2.3 FV Encoding for Low Power Data I/O
Jun Yang, Rajiv Gupta, Univ. of Arizona

P2.4 Time-to-Failure Estimation for Batteries in Portable Electronic Systems
Daler Rakhmatov, Sarma Vrudhula, Univ. of Arizona

P2.5 Architecture Strategies for Energy Efficient Packet Forwarding in Wireless Sensor Networks
Vlasios Tsiatsis, Scott Zimbeck, Mani Srivastava, UCLA

P2.6 Modulation Scaling for Energy Aware Communication Systems
Curt Schurgers, Olivier Aberthorne, Mani Srivastava, UCLA

12:15-13:30 Buffet Lunch and Poster Discussions
Pacific Room A-B

13:30-14:15 Invited Talk 1 ***Waterfront Ballroom A-B-C***
Session Chair: Murli Tirumala, Intel

Cooling and Power Considerations for Semiconductors into the Next Century
Christian Belady, Hewlett Packard

14:30-16:00 Session 3: ***Waterfront Ballroom A-B***
Low Power RF Circuits and Systems
Session Chair: Frank Chang, UCLA
Session Organizer: Vickram Vathulya, Philips Research

3.1 Energy Efficient Modulation and MAC for Asymmetric RF Microsensor Systems
Andrew Wang, SeongHwan Cho, Charles Sodini, Anantha Chandrakasan, MIT

3.2 A 1V, 1.9GHz Mixer using a Lateral Bipolar Transistor in CMOS
Song Ye, Univ. of Toronto, Koji Yano, Yamanashi Univ., Andre Salama, Univ. of Toronto

3.3 A 60dB, 246MHz CMOS Variable Gain Amplifier for Subsampling GSM Receivers
Mohamed Mostafa, Texas A&M, Sherif Embabi, TI, Mostafa Elmala, Texas A&M

14:30-16:00 Session 4: ***Waterfront Ballroom C***
Modeling and Estimation Techiques
Session Chair: Wolfgang Nebel, Univ. of Oldenburg
Session Organizer: Radu Marculescu, CMU

4.1 VTCMOS Characteristics and Its Optimum Conditions Predicted by a Compact Analytical Model
Hyunsik Im, Takashi Inukai, H. Gomyo, Toshiro Hiramoto, Takayasu Sakurai, Univ. of Tokyo

4.2 Memory Controller Policies for DRAM Power Management
Xiaobo Fan, Carla Ellis, Alvin Lebeck, Duke Univ.

4.3s Run-Time Power Estimation in High Performance Microprocessors
Russ Joseph, Margaret Martonosi, Princeton Univ.

4.4s Fast, Flexible, Cycle-Accurate Energy Estimation
Phillip Stanley-Marbell, Michael Hsiao, Rutgers Univ.

16:00-16:15 Coffee Break

16:15-17:45 Session 5: ***Waterfront Ballroom A-B***
Low Power Digital Circuits
Session Chair: Borivoje Nikolic, UC Berkeley
Session Organizer: Tadahiro Kuroda, Keio Univ.

5.1 Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed FFs for High Performance Microprocessors
James Tschanz, Siva Narendra, Zhanping Chen, Shekhar Borkar, Vivek De, Intel, Monoj Sachdev, Univ. of Waterloo

5.2 Theory and Practical Implementation of Harmonic Resonant Rail Drivers
Joong-Seok Moon, Peter Beerel, USC, William Athas, Apple Computer

5.3s A Resonant Clock Generator for Single-Phase Adiabatic Systems
Conrad Ziesler, Marios Papaefthymiou, Univ. Michigan, Suhwan Kim, IBM

5.4s Enhanced MTCMOS Circuits using Variable Well Biasing
Stephen Kosonocky, Mike Immediato, Peter Cottrell, Terence Hook, Randy Mann, Jeff Brown, IBM

16:15-17:45 Session 6: ***Waterfront Ballroom C***
Bus Encoding
Session Chair: Masahiro Asada, Univ. of Tokyo
Session Organizer: Renu Mehra, Clearwater Networks, Inc.

6.1 Encodings for High Performance Energy-Efficient Signaling
Allessandro Bogliolo, Univ. di Ferrara

6.2 Low Energy Encoding for Deep Submicron Address Buses
Luca Macchiarulo, Enrico Macii, Massimo Poncino, Politecnico di Torino

6.3s Irredundant Address Bus Encoding for Low Power
Yazdan Aghaghiri, Massoud Pedram, USC, Farzan Fallah, Fujitsu Labs

6.4s Low Power Address Encoding using Self-Organizing Lists
Mahesh Mamidipaka, Dan Hirschberg, Nikil Dutt, UC Irvine

17:55-18:25 Session DC ***Waterfront Ballroom A-B***
Design Contest Chair: Vivek Tiwari, Intel

DC1 Energy Efficient High Speed CMOS Links using Adaptive Power Supply Regulation
Jaeha Kim, Mark Horowitz, Stanford

DC2 Dynamically Programmable Parallel Processor: A Novel Architecture with CDMA Bus Interface
Boon-Keat Tan, Ryuji Yoshimura, T. Matsuoka, Osaka Univ.

DC3 A Low Swing Clock Double Edge-Triggered FF
Chulwoo Kim, Sung-Mo Kang, UIUC

DC4 Design Methodolofy for an Integrated Ultra Low Power CMOS Receiver
Shahram Mahdavi, H. Darabi, A. Abidi, UCLA

DC5 A 90Mdb 64 State 130mW 0.35 um CMOS Low Power Viterbi Decoder
Tobias Gemmeke, Oliver Weib, Tobias Noll, RWTH Aachen

19:00-22:00 Reception and Banquet

TUESDAY, August 7, 2001

8:00-9:00 Continental Breakfast

9:00-9:45 Invited Talk 2 ***Waterfront Ballroom A-B-C***
Session Chair: Ingrid Verbauwhede, UCLA

Wireless Sensor Networks: Application Driver for Low Power Distributed Systems
Deborah Estrin, UCLA

9:45-10:00 Coffee Break

9:45-16:45 Exhibits ***Waterfront Ballroom D-E***

10:00-11:30 Session 7: ***Waterfront Ballroom A-B***
Technology for Low Power
Session Chair: Fari Assaderaghi, SiliconWave
Session Organizer: Rajiv Joshi, IBM

7.1 Scaling of Stack Effect and its Application for Leakage Reduction
Siva Narendra, Shekhar Borkar, Vivek De, Dimitri Antoniadis, Intel, Anantha Chandrakasan, MIT

7.2 VTCMOS in Series Connected Circuits
Takashi Inukai, Toshiro Hiramoto, Takayasu Sakurai, Univ. of Tokyo

7.3s Effectiveness of Reverse Body Bias for Leakage Control in Scaled Dual Vt CMOS ICs
A. Keshavarzi, S. Ma, Siva Narendra, B. Bloechel, K. Mistry, T. Ghani, Shekhar Borkar, Vivek De, Intel

7.4s Double-Gate Fully Depleted SOI Transistors for Low Power High Performance Nano-Scale Circuit Design
Rongtian Zhang, Kaushik Roy, David James, Purdue Univ.

10:00-11:30 Session 8: ***Waterfront Ballroom C***
Architectural Techniques
Session Chair: Sumit Roy, Cadence
Session Organizer: Massimo Poncino, Politecnico di Torino

8.1 A Self-Optimizing Embedded Microprocessor using a Loop Table for Low Power
Frank Vahid, Ann Gordon-Ross, UC Riverside

8.2 Low Power Pipelining of Linear Systems: A Common Operand Centric Approach
Daehong Kim, Kiyoung Choi, Seoul National Univ., Dongwan Shin, UC Irvine

8.3s A System Level Energy Minimization Approach using Datapath Width Optimization
Yun Cao, Hiroto Yasuura, Kyushu Univ.

8.4s Energy Efficient Instruction Dispatch Buffer Design for Superscalar Processors
Gurhan Kucuk, Kanad Ghose, Dmitry Ponomarev, SUNY Binghamton, Peter Kogge, Univ. of Notre Dame

11:40-12:15 Poster Session 3 ***Waterfront Ballroom A-B***
Session Chair: Sudhir Gowda, IBM

P3.1 High Density Capacitance Structures in Submicron CMOS for Low Power RF Applications
Tirdad Sowlati, Vickram Vathulya, Domine Leenaerts, Philips Research

P3.2 A CMOS VCO Architecture Suitable for Sub-1 Volt High Frequency RF Applications
Ahmed Mostafa, Mourad El-Gamal, McGill Univ.

P3.3 A Low Power Direct Sequence Spread Spectrum Modem Architecture
Charles Chien, Igor Elgorria, Rockwell Research, Chuck McConaghy, LLNL

P3.4 Effects of Elevated Temperature on Tunable Near-Zero Threshold CMOS
Vjekoslav Svilan, Leonard Tyler, Stanford, James Burr, Sun

P3.5 A Sub-1 Volt Dual Threshold Domino Circuit using Product-of-Sum Logic
Koji Fujii, Takakuni Douseki, Yuichi Kado, NTT

P3.6 Mixed Multi-Threshold Differential Cascode Voltage Switch Circuit Styles and Strategies for Low Power VLSI Design
W. Chen, W. Hwang, P. Kudva, G. Gristede, Steve Kosonocky, Rajeev Joshi, IBM

P3.7 Selectively Clocked Skewed Logic: A Robust Low Power Logic Style for High Performance Applications
Naran Sirisantana, Aiqun Cao, Shawn Davidson, Cheng-Kok Koh, Kaushik Roy, Purdue Univ.

11:40-12:15 Poster Session 4 ***Waterfront Ballroom C***
Session Chair: Giovanni DeMicheli, Stanford

P4.1 A Profile-Based Energy Efficient Intra-Task Voltage Scheduling Algorithm for Hard Real-Time Applications
Dongkun Shin, Jihong Kim, Seoul National Univ.

P4.2 Compiler Directed Dynamic Voltage/Frequency Scheduling for Energy Reduction in Microprocessors
Chung-Hsing Hsu, Ulrich Kremer, Michael Hsiao, Rutgers

P4.3 Variable Voltage Task Scheduling Algorithms for Minimizing Energy
Ali Manzak, Chaitali Chakrabarti, Arizona State Univ.

P4.4 Design Methodology and Optimization Strategies for Dual Vth Schemes using Commercially Available Tools
Masayuki Hirabayashi, Koichi Nose, Takayasu Sakurai, Univ. of Tokyo

P4.5 Synthesis of Low Leakage PD-SOI Circuits with Body-Biasing
Mario Casu, Gianluca Masera, Guido Piccinini, Maurizio Zamboni, Politecnico di Torino

P4.6 Low Power Technology Mapping for Mixed-Swing Logic
Nicola Dragone, Rob Rutenbar, Richard Carley, CMU, Roberto Zafalon, ST Microelectronics

P4.7 A Frequency-Domain Supply Current Macro-Model
Srinivas Bodapati, UIUC, Farid Najm, Univ. of Toronto

12:15-13:30 Buffet Lunch and Poster Discussions
Pacific Room A-B

13:30-15:00 Session 9: *Waterfront Ballroom A-B*
Low Power Analog Techniques
Session Chair: Sudhir Gowda, IBM
Session Organizer: Ken Yang, UCLA

9.1 A Low Power, 5-70 MHz, 7th Order Filter with Programmable Boost, Group Delay, and Gain using Instantaneous Companding
Rola Baki, Mourad El-Gamal, McGill Univ.

9.2s Optimizing Bias Circuit Design of Cascode Operational Amplifiers for Wide Dynamic Range Operations
Takeshi Fukumoto, Hiroyuki Okada, Kazuyuki Nakamura, NEC

9.3s Leakage Current Cancellation Techniques for Low Power Switched-Capacitor Circuits
Louis Wong, Shohan Hossain, Andre Walker, St. Jude Medical

9.4 A 3-Pin 1.5V 550uW 176x144 Self Clocked CMOS Active Pixel Image Sensor
Kwang-Bo Cho, Alexander Krymski, Eric Fossum, Photobit

13:30-15:00 Session 10: *Waterfront Ballroom C*
Algorithmic Transformations and Caching
Session Chair: T.N. Vijaykumar, Purdue
Session Organizer: Babak Falsafi, CMU

10.1 Cached Code Compression for Energy Minimization in Embedded Processors
Luca Benini, Univ. di Bologna, Alberto Macii, Politecnico di Torino, Alberto Nannarelli, Univ. di Roma

10.2 Energy Efficient Turbo Decoding for 3G Mobile
David Garrett, Bing Xu, Chris Nicol, Lucent Technologies

10.3s Low Power AEC-Based MIMO Signal Processing for Gigabit Ethernet 1000 Base-T Transceivers
Lei Wang, Naresh Shanbhag, UIUC

10.4s Power Reduction Through Work Reuse
Emil Talpes, Diana Marculescu, CMU

15:00-15:15 Coffee Break

15:15-16:45 Session 11: *Waterfront Ballroom A-B*
Low Power Digital Building Blocks
Session Chair: David Garrett, Lucent Technologies
Session Organizer: Donald Steiss, Mindspring

11.1 Clocking Strategies and Scannable Latches for Low Power Applications
V. Zyuban, D. Meltzer, IBM

11.2 An Ultra Low Power DLMS Adaptive Filter for Hearing Aid Applications
Hyung-Il Kim, Kaushik Roy, Purdue Univ.

11.3s A Dynamic SDRAM Mode Control Scheme for Low Power Systems with a 32-bit RISC CPU
Seiji Miura, Kazushige Ayukawa, Takao Watanabe, Hitachi

11.4s Analysis and Implementation of Charge Recycling for Deep Submicron Buses
Paul Sotiriadis, Theodoros Konstantakopoulos, Anantha Chandrakasan, MIT

15:15-16:45 Session 12: *Waterfront Ballroom C*
Power Supply and Delivery
Session Chair: Farid Najm, Univ. of Toronto
Session Organizer: Ed Huijbregts, Magma

12.1 Estimation of Power Distribution in VLSI Interconnects
Youngsoo Shin, Takayasu Sakurai, Univ. of Tokyo

12.2 Maximum Voltage Variation in the Power Distribution Network of VLSI Circuits with RLC Models
Sudhakar Bobba, Sun, Ibrahim Hajj, American Univ. of Beirut

12.3s Battery Capacity Measurement and Analysis using Lithium Coin Cell Batteries
Sung Park, Andreas Savvides, Mani Srivastava, UCLA

12.4s On the Interaction of the Power Distribution Network with the Substrate
Rajendran Panda, Savithri Sundareswaran, David Blaauw, Motorola