Next-Generation Power-Aware Design

Prof. Takayasu Sakurai
Institute of Industrial Science,
University of Tokyo
E-mail: tsakurai@iis.u-tokyo.ac.jp
We can help in two ways for “Cool Earth”

- Green of IT

- Green by IT
Next-Generation Power-Aware Design

- 3D integration
- Deep sub-volt design
- Organic integrated circuits (Green by IT)
Power distribution is diverse

Chart showing the distribution of logic, memory, and I/O for MPU1, MPU2, ASSP1, and ASSP2.
System-on-a-Chip reduces I/O power but...

Separate chips

Logic & memory

DRAM - logic interface

Power

DRAM on a chip

240mW

891mW

70% power reduction by DRAM embedding but expensive.

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3D achieves low power and high performance with reasonable cost

2D assembly

More devices in closer vicinity

Reducing R and C

Lower power
Higher performance

Substrate < 20µm thick

3-D SiP

8 times more devices in 1mm distance

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Stacked processor & cache by processor companies

Heat sink from back of processor

Processor, 1TFLOPS at 98W
22 mm x 13.75 mm
80 cores, face down
Each unit is core + router

Stacked memory
256KB SRAM per core
4x C4 bump density
8490 through-Si vias

Package

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New contender – wireless link

Capacitive and inductive-coupling links
Wireless data links between stacked chips
No need for additional wafer process ➔ low cost
No need for ESD protection circuit ➔
high speed + low power

Metal Electrode
Capacitive-Coupling Link
U. Tokyo and Keio U., (ISSCC’03)

Metal Coil
Inductive-Coupling Link
Keio U. and U. Tokyo, (ISSCC’04)
How were we and how are we?

Inductive Wireless Superconnect
Connecting multiple chips


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120µm coils couple through stacked chips

Transmitter (Top Chip)

Fabricated in 180nm CMOS

Top Chip
(40,25,10µm-Thick)

Distance=45,30,15µm

Receiver (Bottom Chip)

Bottom Chip

Voltage supply by bonding does not increase power nor decrease speed.

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Just talk without waiting for clock - fast

<table>
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<th>Circuit Topology</th>
<th>Keio U. / U. Tokyo (ISSCC’07)</th>
<th>Proposed Transceiver</th>
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<td><strong>Synchronous front-end</strong></td>
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<td>Txclk</td>
<td><strong>Pulse Generator</strong></td>
<td>H-Bridge</td>
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<td>Long Latency</td>
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<td><strong>Timing Controller</strong></td>
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<td><strong>Asynchronous front-end</strong></td>
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<tr>
<td>Txdata</td>
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<tr>
<td>Rxdata</td>
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<table>
<thead>
<tr>
<th>Data Rate</th>
<th>1Gb/s</th>
<th>11Gb/s</th>
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<tr>
<td>Latency</td>
<td>600ps</td>
<td>36ps</td>
</tr>
<tr>
<td>Energy/bit</td>
<td>0.4pJ/b</td>
<td>1.4pJ/b</td>
</tr>
</tbody>
</table>

Simulated in 180nm CMOS

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High-Speed Inductive-Coupling Link

Transmitter

Receiver

Txdata   Txdata

Rxdata   Rxdata

$V_R$  $V_B$

$I_T$

$1.5$

$0$

$-1.5$

$4$

$0$

$-4$

$100$

$0$

$-100$

$0.5$

$0$

$-0.5$

$0$

$0.5$

$1$

$1.5$

Time [ns]

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11Gbps over 15μm Measured

BER vs. Data Rate [Gb/s]

Communication Distance, X

Inductive-Coupling Link

Tx ↔ Rx

X = 15μm
X = 30μm
X = 45μm

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## Lower power solution in scaled CMOS

### Multiple Use of Data Links with 400MHz System Clock

<table>
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<th>90nm CMOS (Simulated)</th>
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<tr>
<td>Link</td>
<td>11Gb/s</td>
<td>30Gb/s</td>
</tr>
<tr>
<td>Burst</td>
<td>6.4Gb/s</td>
<td>20.8Gb/s</td>
</tr>
<tr>
<td><strong>Energy</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Link</td>
<td>1.4pJ/b</td>
<td>0.11pJ/b ~0.03pJ/b @ 45nm</td>
</tr>
<tr>
<td>Burst</td>
<td>52.6pJ/b</td>
<td>11.2pJ/b</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel*</td>
<td>0.3mm² (16Links for 6.4Gb/s)</td>
<td>0.96mm² (52Links for 20.8Gb/s)</td>
</tr>
<tr>
<td>Burst</td>
<td>0.1mm² (2Links for 6.4Gb/s)</td>
<td>0.08mm² (2Links for 20.8Gb/s)</td>
</tr>
<tr>
<td><strong>Area Reduction by Burst Transmission</strong></td>
<td>1/3</td>
<td>1/12</td>
</tr>
</tbody>
</table>

*Multiple Use of Data Links with 400MHz System Clock

For TSV connection:

\[
E = PD = \frac{fCV^2}{f} = CV^2 \sim C \text{ (V\sim1)} = 0.03pJ/b \text{ (w/ ESD)}
\]

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L-coupled link: low power contender

EMI? Near Field and Far Field

Communication Distance: $x$

Signal Frequency: $f$ [Hz]

- Chip-link in SiP
- Near Field (Reactive)
- Far Field (Radiative)
- mm-Wave
- WLAN
- Cellular
- RFID (135kHz)
- RFID (13.56MHz)
- RFID (2.4MHz)
- FM

$f = \frac{c}{2\pi x}$, $x = \lambda/2\pi$


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It’s not paradise: remaining issues for 3D SiP

- **KGD (Known Good Die)**
  At-speed testing of wafer, Wafer burn-in, Huge pin counts

- Heat removal and inspection of contacts
  Heat estimate, Testing by X-ray and ultrasonic

- Interposer
  Secure power distribution circuits, RLC testing

- Design environments
  EMC, Noise, Heat, 3D modeling, Simulation

- Standardization
  Protocol, Electrical, Physical, Testing, Logistics, Legal issues, 3D data handling

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3D SiP house

Foundry A

Foundry B

Foundry C

Foundry may provide TSV service.

TSV / wireless

KGD test

Interposer, Assembly & test

KGD test

TSV by 3D SiP house is based on “Via-last”

3D SiP to system customer

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Interposer to ensure design freedom

Foundry A
Foundry A
TSV’ed memory can be considered as one LSI product.

Assembly-specific
Re-distribution layer to adjust TSV location and material discrepancy among dies.

Foundry A or B
May experience separate shrink and multi-vendor supply.

Silicon/glass or organic depends on design rule (~10µm) and cost trade-off

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Future power-aware 3D integration

Stacked memories

- Power unit
- Proc. unit
- Specialized blocks
- Sensors and information collecting circuits
- HV Power grid
- Stacked analog/RF, HV, sensors, MEMS...

Next-Generation Power-Aware Design

- 3D integration
- Deep sub-volt design
- Organic integrated circuits (Green by IT)
Ultra-low voltage domain

Normalized delay & power

Simulation (fitted to measurement)

Normalized PD product

Normalized delay & power

V_{DD} [V]

PD product

Power

Delay

Normalized PD product
Ring Oscillators to enable $V_{DD\min}$ Measurement

- $V_{DD2}$-$V_{SS2}$ of output buffer is separated from $V_{DD2}$-$V_{SS2}$ of ring oscillator, so that small swing output signal can be measured.

- NMOS/PMOS body bias voltage of ring oscillators can be tuned independently.

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Fabricated Ring Oscillators (RO’s)

- 90nm CMOS process, based on standard cell library
- Three RO’s (11-stage, 101-stage and 1001-stage)
- More stages up to million gates in subsequent tapeout

$V_{DD_{min}}$ simulation

Diagram showing the behavior of $V_{OUT}$ over time and the relationship between $V_{OUT}$ and $V_{DD_{min}}$. The graph plots voltage (in mV) against time (in µs) over a simulation period.
$V_{DD}$ Dependence of Oscillation Frequency

- $V_{DD\text{min}}$ is defined as the supply voltage when the RO's stop oscillation and no voltage transition from the output buffer are observed.
- $V_{DD\text{min}}$ of 11-stage ring oscillator is lower than that of 1001-stage ring oscillator.
Measured Die-to-Die (D2D) variations

Frequency variations increase with reduced $V_{DD}$.

- $\Delta f = \frac{\Delta t_{pd}}{t_{pd}} \frac{\alpha}{V_{DD} - V_{TH}} \Delta V_{TH}$
- $t_{pd} \propto \frac{C V_{DD}}{(V_{DD} - V_{TH})^\alpha}$
The spatial spectrum doesn’t show distinctive peaks at particular spatial frequencies, which indicates that the intra-die $V_{TH}$ variations are not systematic but purely random across 4mm.

What’s happening at $V_{DD_{min}}$

$V_{DD}=85\text{mV}$

Fail

$V_{OUT\_LOW\_7} > V_{INV\_8}$
Adaptive body bias to reduce $V_{DDmin}$

The body bias of pMOS is adaptively controlled to minimize $V_{DDmin}$ and the body bias of nMOS is fixed.

When a common body bias is applied to the 11 inverters, $V_{DDmin}$ improvement is only 2mV.
Fine-grained body bias to reduce $V_{DD\text{min}}$

- $V_{DD\text{min}} = 85$ mV
- $V_{DD\text{min}} = 43$ mV

When independent body bias is applied for every 2 inverters, $V_{DD\text{min}}$ improvement is only 4mV.

When inverter-by-inverter body bias is applied, $V_{DD\text{min}}$ is drastically reduced to 43mV. But it is impractical.

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Worst-case distribution

Largest value distribution of n variables, each following Gaussian distribution

\[
f(x) = \frac{1}{\sqrt{2\pi \sigma}} e^{-\frac{(x-x_0)^2}{2\sigma^2}}
\]

\[
\frac{d}{dx}\left(\int_{-\infty}^{x} \frac{1}{\sqrt{2\pi \sigma}} e^{-\frac{(y-x_0)^2}{2\sigma^2}} dy \right)^n
\]

SD \sim \frac{1}{(\log_10 n + 1)^{1.4} \sigma} = \frac{1}{(k+1)^{1.4} \sigma} (if \ n = 10^k)

peak \sim \bar{x} + 2\sqrt{k} \sigma (if \ n = 10^k)

\sim \bar{x} + 2\sqrt{\log_{10} n} \sigma
$V_{DDmin}$ of million-stage ring oscillator

Center $V_{TH}=0.22V$

Model calculation

Worst case $\sim \bar{x} + 2\sqrt{\log_{10} n} \sigma$


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Next-Generation Power-Aware Design

- 3D integration
- Deep sub-volt design
- Organic integrated circuits (Green by IT)
Frequently-mentioned features of organic IC’s

- **Advantages**
  - Low-cost manufacturing
  - Mechanical flexibility

- **Disadvantages**
  - Low speed (<10^{-3} of Si VLSI)
  - Low density (<10^{-4} of Si VLSI)
Cost consideration

- **Cost per function**
  (processors, memories, analog, ...)

- **Cost per area**
  (sensors, display, actuators, ...)

**Organic**

**Si**

Good for Green by IT

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Unique manufacturing process: Printing large-area organic transistor array
Screen printing
Epoxy partitions

Courtesy of Professor Takao Someya, University of Tokyo
Inkjet printing

Gate electrodes & Word line

Gate electrodes: 45 x 45
Word line: 45 lines

28 x 28 cm²

3 mm
Organic transistors

Organic semiconductors: main elements --- C & H

Pentacene

Source
Gate
Drain

OFF

ON

Current

Voltage
Modeling by SPICE level1

L=100μm, W=2mm

V_{GS} =
-40V
-30V
-20V
-10V

I_{DS} [µA]

V_{DS} [V]

Measurement
Simulation

Level 1 SPICE
MOS model

SPICE & VLSI layout tool work.

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Large-area electronics

Human-scale interfaces

E-skin

Sheet scanner

Braille display

Power sheet

Comm sheet

IEDM’03
IEDM’04
IEDM’05
IEDM’06
IEDM’07
ISSCC’04
ISSCC’05
ISSCC’06
ISSCC’07
ISSCC’08
Pressure sensors + OFETs
Actuators + OFETs
Photodetectors + OFETs
Coils + MEMS + OFETs
Organics + Si co-design

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Large-area & high efficiency

**Large coil**
- 30x30 cm² x 1 coil
- Efficiency ~ 0.1%
- Electro-magnetic induction works

**Receiver coil**
- 1 inch²
- Efficiency > 60%
- Selective activation is the key.

**Many coils**
- & one selected

**Receiver coil**
- 1 inch²

1 inch² x 64 coils

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Combination of MEMS and OFET

- Power transmission coils
- Plastic MEMS switches
  - Low loss
  - Slow ~ 0.1s
  - # of switching limited

- Position-sensing coils
- Organic FETs
  - Resistive
  - Faster < ms
  - # of switching unlimited

- Wireless power transmission system
- Contactless position-sensing system

21 x 21 cm² (8 x 8 cells)

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MEMS switches

~ 5mm x 10mm

Electrode for power transmission

Electrode for electrostatic attraction
Wireless power transmission sheet

- Large-area & Low cost
- Contactless position sensing
- High power
- Lightweight & Printable

Size: 21 x 21 cm²
Thickness: 1 mm
Weight: 50 g
Efficiency: 62.3%
Max received power: 29.3 W
X’mas tree w/o a battery wirelessly powered

21 LEDs
13.56 MHz
Received power : 2 W
Demonstration of power transmission (Ubiquitous electronics)

In the wall
TV on a wall
Mobile phone & PC & e-accessories
(data can be wireless but USB’s wire delivers power)

In the table
Home-care robot
Vacuum cleaner

In the floor
Ambient illumination
No electrical shock

I touched it by my hand. No problem 😊
Next-Generation Power-Aware Design

- 3D integration
  Wireless link \((0.17 \text{pJ/b} \rightarrow 0.03 \text{pJ/b})\)
- Deep sub-volt design
  Watch out for random WID variation
- Organic integrated circuit
  Large-area electronics for Green by IT

All can help to realize COOL EARTH through “Green of IT” and “Green by IT”.

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