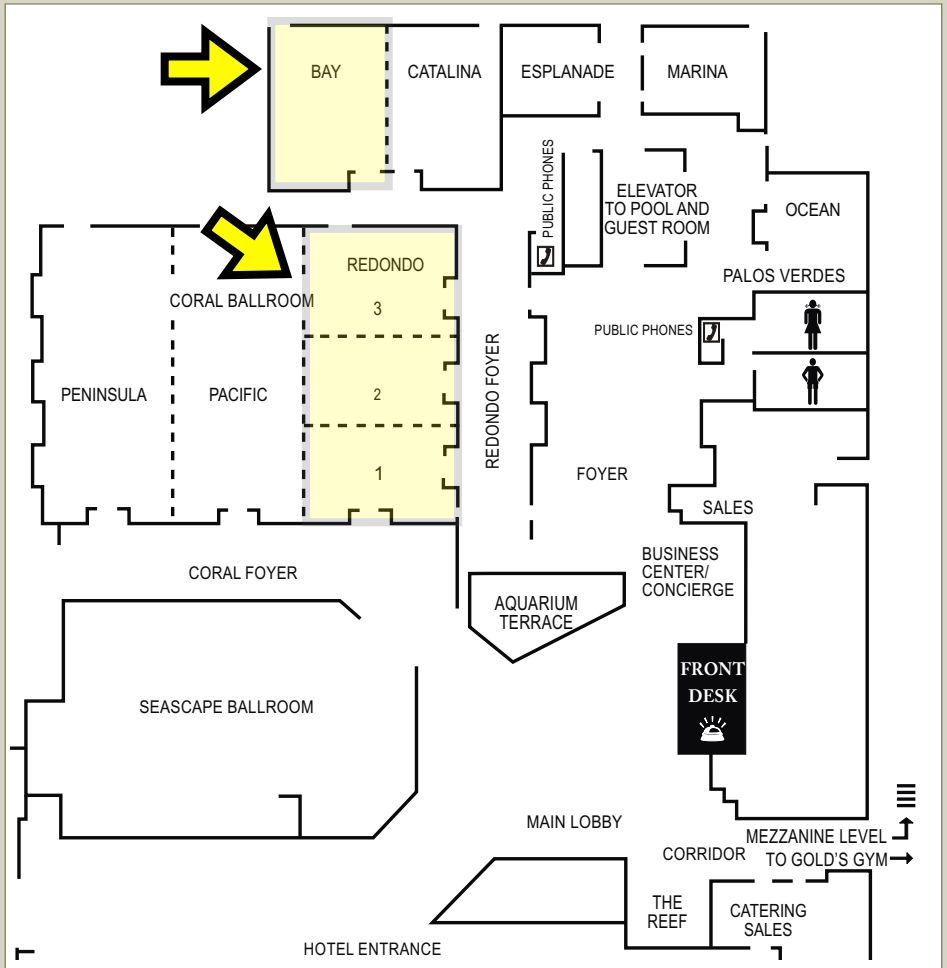

Meeting Rooms

The meeting rooms are Bay Room and Redondo Room. The plenary sessions are held in Redondo Room.

ISLPED'12

Crowne Plaza Hotel
Redondo Beach, CA
July 30-Aug. 1, 2012
(reception Sunday evening)

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ISLPED 2012
Program at a Glance

Sunday, July 29, 2012

Time	Bay Room	Redondo Room
18:00	Reception	

Monday, July 30, 2012

Time	Bay Room	Redondo Room
7:00	Breakfast	
8:00	Chairs' Welcome	
8:30	Keynote by Pradip Bose, IBM "Energy Secure Computing"	
9:30	Break	
10:00	Session 1: Circuits in Emerging Techniques	Session 2: Tools for Physical Design and Architecture Simulation
11:30	Lunch	
13:00	Session 3: Caches, Memories, and Interconnect	Session 4: Industry FOcus Session on Low Power Design
15:00	Break	
15:30	Session 5: Low Power SRAM	Session 6: System Level Power Optimization
17:00	Session 8: Low Power Design and Validation Methodologies	Session 7: Panel - Going Green Across Communication and Storage Subsystems
18:30	(free activity)	

Tuesday, July 31, 2012

Time	Bay Room	Redondo Room
7:00	Breakfast	
8:00	Keynote by Kaushik Roy, Purdue U. "Spin as State Variable for Computation: Prospects and Perspectives"	
9:00	Break	
9:30	Session 9: Digital Techniques	Session 10: Energy Efficiency and Non-Volatile Memories
11:30	Poster Session	
12:00	Lunch	
13:30	Session 11: Innovations in Low Power Analog	Session 12: Software-Driven Techniques for Energy Efficiency in Embedded Multi-Core Systems
15:30	Break	
16:00	Design Contest	Embedded Tutorial
17:30	Industry Reception	
19:00	Social Event - Banquet	

Wednesday, August 1, 2012

Time	Bay Room	Redondo Room
7:30	Breakfast	
8:30	Keynote by Uming Ko, MediaTek USA, "Ultra-Low Power Challenges for the Next Generation ASIC"	
9:30	Break	
10:00	Session 13: Processor Design and Implementation	Session 14: Memory Management and Scheduling

Monday, July 30, 2012 (1/2)

Time	Bay Room	Redondo Room
7:00	**Breakfast**	
8:00	**Chairs' Welcome** (Bay Room)	
8:30	**Keynote:** *Energy Secure Computing* - Speaker: Pradip Bose, IBM Chair: Massimo Poncino, Politecnico di Torino	
9:30	**Break**	
10:00 - 11:30	**Session 1: Circuits in Emerging Techniques** Chair: Kangho Lee (Qualcomm), Co-Chair: Jae-Joon Kim (IBM)	**Session 2: Tools for Physical Design and Architecture Simulation** Chair: Houman Homayoun (George Mason U)
10:00	★ *Write-Optimized Reliable Design of STT MRAM* Yusung Kim, Sumeet Gupta, Sang Phill Park, Georgios Panagopoulos, Kaushik Roy (Purdue U)	*Practically Scalable Floorplanning with Voltage Island Generation* Song Chen, Xiaolin Zhang, Takeshi Yoshimura (Waseda U)
10:30	*High-Performance Low-Energy STT MRAM Based on Balanced Write Scheme* Dongsoo Lee, Sumeet Gupta, Kaushik Roy (Purdue U)	★ *TSV Array Utilization in Low-Power 3D Clock Network Design* Xin Zhao, Sung Kyu Lim (Georgia Institute of Technology)
11:00	*Design Benchmarking to 7nm with FinFET Predictive Technology Models* Saurabh Sinha, Brian Cline, Greg Yeric, Vikas Chandra (ARM); Yu Cao (Arizona State U)	*Thermal-Aware Sampling in Architectural Simulation* Ehsan K. Ardestani, Elnaz Ebrahimi, Gabriel Southern, Jose Renau (UC Santa Cruz)
11:30	**Lunch**	
13:00 - 15:00	**Session 3: Caches, Memories, and Interconnect** Chair: Saurabh Sinha (ARM), Co-Chair: Xiangyu Dong (Qualcomm)	**Session 4: Industry Focus Session on Low Power Design** Chair: Clive Bittlestone (Texas Instruments)

Time	Bay Room	Redondo Room
13:00	★ *ER: Elastic RESET for Low Power and Long Endurance MLC based Phase Change Memory* Lei Jiang, Youtao Zhang, Jun Yang (U of Pittsburgh)	*Advances in Ultrabook™ Platform Power Management* Jim Kardach (Intel Corp.)
13:30	*A Dual-mode Architecture for Fast-switching STT-RAM* Zhenyu Sun, Hai (Helen) Li (Polytechnic Institute of New York U); Wenqing Wu (Qualcomm Inc)	*Commercial Low-Power EDA Tools: A Review* Renu Mehra (Synopsys)
14:00	*ASCIB: Adaptive Selection of Cache Indexing Bits for Removing Conflict Misses* Alberto Ros (Universidad de Murcia); Polychronis Xekalakis (Intel Labs Barcelona); Marcelo Cintra (The University of Edinburgh); Manuel E. Acacio, José M. García (Universidad de Murcia)	*An ARM perspective on Addressing Low-Power Energy-Efficient SoC Designs* David Flynn (ARM)
14:30	*Energy Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Systems* Jieming Yin, Pingqiang Zhou, Anup Holey, Sachin S. Sapatnekar, Antonia Zhai (U of Minnesota, Twin Cities)	*Panel* Moderator: Ajith Amerasekera (TI) Panelists: Barry Pangrle (Mentor), Jim Kardach (Intel); RenuMehra (Synopsys), David Flynn (ARM)
15:00	**Break**	
15:30 - 17:00	**Session 5: Low Power SRAM** Chair: Min Huang (Intel), Co-Chair: Srini Sridhara (Texas Instruments)	**Session 6: System Level Power Optimization** Chair: Yung-Hsiang Lu (Purdue), Co-Chair: Ayse K. Coskun (Boston Univ.)

★ *best-paper candidate*

Monday, July 30, 2012 (2/2)

Time	Bay Room	Redondo Room
15:30	*A 55nm 0.55V 6T SRAM with Variation-Tolerant Dual-Tracking Word-Line Under-Drive and Data-Aware Write-Assist* Yi-Wei Lin, Hao-I Yang, Geng-Cing Lin, Chi-Shin Chang, Ching-Te Chuang, Wei Hwang (National Chiao Tung U); Chia-Cheng Chen, Willis Shih, Huan-Shun Huang (Faraday Technology)	*Power-aware Performance Increase via Core/Uncore Reinforcement Control for Chip-Multiprocessors* Da-Cheng Juan, Diana Marculescu (CMU)
16:00	*A 40-nm 256-Kb Sub-10 pJ/Access 8T SRAM with Read Bitline Amplitude Limiting (RBAL) Scheme* Shusuke Yoshimoto, Masaharu Terada, Youhei Umeki, Shunsuke Okumura (Kobe University); Atsushi Kawasumi, Toshikazu Suzuki, Shinichi Moriwaki, Shinji Miyano (STARC); Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe U)	*Power Conversion Efficiency Characterization and Optimization for Smartphones* Woojoo Lee, Yanzhi Wang (U of Southern California); Donghwa Shin, Naehyuck Chang (Seoul National U); Massoud Pedram (USC)
16:30	*An Adaptive Write Word-Line Pulse Width and Voltage Modulation Architecture for Bit-Interleaved 8T SRAMs* Daeyeon Kim (U of Michigan); Vikas Chandra, Robert Aitken (ARM); David Blaauw, Dennis Sylvester (U of Michigan)	*Dynamic Reconfiguration of Photovoltaic Energy Harvesting System in Hybrid Electric Vehicles* Yanzhi Wang, Xue Lin (USC); Naehyuck Chang (Seoul National U); Massoud Pedram (USC) *Battery Management for Grid-connected PV Systems with a Battery* Sangyoung Park (SNU); Yanzhi Wang (USC); Younghyun Kim, Naehyuck Chang (SNU); Massoud Pedram (USC)
17:00 - 18:30	**Session 8: Low Power Design and Validation Methodologies** Chair: Michael Orshansky (UT Autin)	**Session 7: Panel - Going Green Across Communication and Storage Subsystems** Session Chair: Ken Wagner (PMC-Sierra, Inc)

Time	Bay Room	Redondo Room
17:00	*Modeling, Design and Cross-Layer Optimization of Polysilicon Solar Cell Based Micro-scale Energy Harvesting System* Elif Selin Mungan, Chao Lu, Kaushik Roy, Vijay Raghunathan (Purdue U)	Panelists: Martin St. Laurent (Qualcomm, USA) Robert Aitken (ARM, USA) Hugh Barrass (Cisco, USA) Randall Robinson (Rackforce Networks, Canada)
17:30	*Static Low Power Verification Flow at Transistor Level for SoC Design* Jérôme Lescot, Vincent Bligny (STEricsson); Dina Medhat (Mentor Graphics); Didier Chollat-Namy (STEricsson); Ziyang Lu, Sophie Billy, Mark Hofmann (Mentor Graphics)	(panel continued)
18:00	*CCP: Common Case Promotion for Improved Timing Error Resilience with Energy Efficiency* Lu Wan, Deming Chen (University of Illinois at Urbana-Champaign) *Energy-Optimal Caches with Guaranteed Lifetime* Mirko Loghi (University di Udine); Haroon Mahmood, Andrea Calimera, Massimo Poncino, Enrico Macii (Politecnico di Torino)	(panel continued)
18:30	**(Free Activity)**	

Tuesday, July 31, 2012 (1/3)

Time	Bay Room	Redondo Room
7:00	**Breakfast**	
8:00	**Keynote:** Spin as State Variable for Computation: Prospects and Perspectives Speaker: Kaushik Roy, Purdue University Chair: Naresh Shanbhag, UIUC	
9:00	**Break**	
9:30 - 11:30	**Session 9: Digital Techniques** Chair: Nikola Nedovic (Fujitsu), Co-Chair: Steven Bartling (Texas Instruments)	**Session 10: Energy Efficiency and Non-Volatile Memories** Chair: Elaheh Bozorgzadeh (UC Irvine), Co-Chair: John Sartori (UMN)
9:30	*Register File Write Data Gating Techniques and Break-Even Analysis Model* Eric Donkoh, Teck Siong Ong, Yan Nee Too (Intel Corp); Patrick Chiang (Oregon State U)	*Improving Energy Efficiency of Write-Asymmetric Memories by Log Style Write* Guangyu Sun (Peking U.); Yaojun Zhang (UPitt), Yu Wang (Tsinghua U.); Yiran Chen (UPitt)
10:00	*A Low-Leakage Dynamic Register File with Unclocked Wordline and Sub-Segmentation for Improved Bitline Scalability* Eric Donkoh (Intel); Patrick Chiang (OSU)	*Process Variation Aware Data Management for STT-RAM Cache Design* Zhenyu Sun, Xiuyuan Bi, Hai (Helen) Li (Polytechnic Institute of New York U)
10:30	*A Fine-Grained Many V_T Design Methodology for Ultra Low Voltage Operations* Mingoo Seok (Columbia U)	★ *TapeCache: A High Density, Energy Efficient Cache Based on Domain Wall Memory.* Rangharajan Venkatesan, Vivek Kozhikkottu (Purdue); Charles Augustine, Arijit Raychowdhury (Intel); Kaushik Roy, Anand Raghunathan (Purdue)
11:00	*A Programmable Resistive Power Grid for Post-Fabrication Flexibility and Energy Tradeoffs* Kyle Craig (U of Virginia & AMD), Yousef Shakhsheer, Sudhanshu Khanna, Saad Arrabi, John Lach, Benton Calhoun (U of Virginia); Stephen Kosonocky (Advanced Micro Devices)	*A Software Approach for Combating Asymmetries of Non-Volatile Memories* Yong Li, Yiran Chen, Alex K. Jones (UPitt) *Design of Low Power 3D Hybrid Memory by Non-volatile CBRAM-Crossbar with Block-level Data-retention* Yuhao Wang, Chun Zhang, Hao Yu, Wei Zhang (Nanyang Tech. U)

Time	Bay Room	Redondo Room
11:30	**Poster Session** Chair: Antonia Zhai (Univ. of Minnesota), Co-Chair: Yuan Xie (Penn State Univ.)	
	TAP: Token-Based Adaptive Power Gating. Andrew Kahng, Seokhyeong Kang, Tajana Rosing, Richard Strong (UCSD)	
	Design Trade-Offs for High Density Cross-Point Resistive Memory. Dimin Niu, Cong Xu (Penn State Univ.); Naveen Muralimanohar, Norman Jouppi (HP Labs); Yuan Xie (PSU)	
	Performance and Energy-Efficiency Improvement through Modified CPL in Organic Transistor Integrated Circuits. Mingoo Seok (Columbia Univ.)	
	Optimal Power Switch Design for Dynamic Voltage Scaling from High Performance to Subthreshold Operation. Kyle Craig, Yousef Shakhsheer, Benton Calhoun (U. of Virginia)	
	BiN: A Buffer-in-NUCA Scheme for Accelerator-Rich CMPs. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Chunyue Liu, Glenn Reinman (UCLA)	
	Adopting TLB Index-based Tagging to Data Caches for Tag Energy Reduction. Jongmin Lee, Soontae Kim (KAIST)	
	Static and Dynamic Co-Optimizations for Blocks Mapping in Hybrid Caches. Yu-Ting Chen, Jason Cong, Hui Huang, Chunyue Liu, Raghu Prabhakar, Glenn Reinman (UCLA)	
	Design Space Exploration of Workload-specific Last-Level Caches. Karthik Swaminathan, Emre Kultursay, Vinay Saripalli, Vijay Narayanan, Mahmut Kandemir (Penn. State U.)	
	Low-Power Adaptive RF Systems using Real-time Fuzzy Noise-Distortion Control. Debashis Banerjee (Georgia Institute of Technology); Shreyas Sen (Intel); Aritra Banerjee, Abhijit Chatterjee (Georgia Tech.)	
	Designing for Dark Silicon: A Methodological Perspective on Energy Efficient Systems. Jason Allred, Sanghamitra Roy, Koushik Chakraborty (Utah State U.)	
	HANDS: Heterogeneous Architectures and Networks-on-Chip Design and Simulation. Davide Zoni, Simone Corbetta, William Fornaciari (Politecnico di Milano)	

★ *best-paper candidate*

Tuesday, July 31, 2012 (2/3)

Time	Bay Room	Redondo Room
	XIOSim: Power-Performance Modeling of Mobile x86 Cores. Svilen Kanev, Gu-Yeon Wei, David Brooks (Harvard U.)	
	LogStore: Toward Energy-Proportional Storage Servers. Wei Zheng, Ana Paula Centeno (Rutgers U.); Frederic Chong (UCSB); Ricardo Bianchini (Rutgers U.)	
	A Game Theoretic Resource Allocation for Overall Energy Minimization in Mobile Cloud Computing System. Yang Ge, Yukan Zhang, Qinru Qiu (Syracuse U.); Yung-Hsiang Lu (Purdue U.)	
	A Low-power "Near-threshold" Epileptic Seizure Detection Processor with Multiple Algorithm Programmability. Himanshu Markandeya (Purdue U.); Shriram Raghunathan (Cyberonics Inc.); Pedro Irazoqui, Kaushik Roy (Purdue U.)	
	Understanding the Impact of Laptop Power Saving Options on User Satisfaction Using Physiological Sensors. Matthew Schuchhardt, Ben Scholbrock, Utku Pamuksuz, Gokhan Memik, Peter Dinda (Northwestern U.); Robert P. Dick (U. of Michigan)	
	MultiScale: Memory System DVFS with Multiple Memory Controllers. Qingyuan Deng (Rutgers U.), David Meisner (Facebook), Abhishek Bhattacharjee (Rutgers), Thomas F. Wenisch (UMich), Ricardo Bianchini (Rutgers)	
	Semantics-driven Sensor Configuration for Energy Reduction in Medical Sensor Networks James B. Wendt, Saro Meguerdichian, Hyduke Noshadi, Miodrag Potkonjak (UCLA)	
12:00	**Lunch**	
13:30 - 15:30	**Session 11: Innovations in Low Power Analog** Chair: Rajeevan Amirtharajah (UC Davis), Co-Chair: Karthik Kadirvel (Texas Instruments)	**Session 12: Software-Driven Techniques for Energy Efficiency in Embedded and Multi-Core Systems** Chair: Nikil Dutt (UC Irvine), Co-Chair: Vivek Tiwari (Intel)

★ *best-paper candidate*

Time	Bay Room	Redondo Room
13:30	*Voltage Droop Reduction for Multiple-Power Domain SoCs with On-Die LDO Using Output Voltage Boost and Adaptive Response Scaling* Tetsutaro Hashimoto, Satoshi Tanabe, Kouichi Nakayama, Hisanori Fujisawa (Fujitsu Laboratories Limited)	*A Study of the Effectiveness of CPU Consolidation in a Virtualized Multi-Core Server System* Inkwon Hwang, Massoud Pedram (USC); Timothy Kam (Intel)
14:00	★ *A 33μW 42 GOPS/W 64x64 Pixels Vision Sensor with Dynamic Background Subtraction for Scene Interpretation* Nicola Cottini, Massimo Gottardi, Nicola Massari (Fondazione Bruno Kessler); Roberto Passerone (Università di Trento); Zeev Smilansky (Emza Visual Sense Ltd.)	*Energy-Efficient Scheduling on Heterogeneous Multi-Core Architectures* Jason Cong, Bo Yuan (UCLA)
14:30	*Process and Temperature Invariant Bandwidth and Gain, Low-Area, Low-Power and High Swing G_m-C Filter for Multichannel Neuro-potential Signal Conditioning* Anvesha Amaravati, Maryam Shojaei Baghini (IIT-Bombay)	★ *MAC: Migration-Aware Compilation for STT-RAM based Hybrid Cache in Embedded Systems* Qingan Li, Jianhua Li, Liang Shi, Chun Jason Xue (City U. of Hong Kong); Yanxiang He (Wuhan U.)
15:00	*A Charge Pump Based Receiver Circuit for a Voltage Scaled Interconnect Aatmesh Shrivastava, John Lach, Benton* Calhoun (U. of Virginia) *0.35V, 4.1μW, 39MHz Crystal Oscillator Circuit in 40nm CMOS* Akira Saito (STARC); Yunfei Zheng (U. of Tokyo); Kazunori Watanabe (STARC); Takayasu Sakurai, Makoto Takamiya (U. of Tokyo)	*Energy-Efficient Signal Processing in Wearable Embedded Systems: An Optimal Feature Selection Approach* Hassan Ghasemzadeh, Navid Amini, Majid Sarrafzadeh (UCLA)
15:30	**Break**	
16:00	**Design Contest** Co-Chairs: Chia-Lin Yang (National Taiwan U), Yiran Chen (U. of Pittsburgh)	**Embedded Tutorial:** Advanced Power and Thermal Management for Low-Power, High-Performance Smartphones Speaker: Hwisung Jung (Broadcom)

Tuesday, July 31, 2012 (3/3)

Time	Bay Room	Redondo Room
	An Ultra Energy Efficient Nonvolatile Processor for Self-powered Sensor Platforms. Yiqun Wang, Yongpan Liu, Shuangchen Li, Daming Zhang, Hongyang Jia, Huazhong Yang, Mei-fang Chiang, Yan-xin Yan and Baiko Sai (Tsinghua University)	
	A 14.5 fJ/cycle/k-gate ECG Processor in 45 nm CMOS Using Statistical Error Compensation. Rami Abdallah and Naresh Shanbhag (UIUC)	
	First-Generation Hybrid Electrical Energy Storage System. Younghyun Kim, Donghwa Shin, Jaehyun Park, Youngil Kim, Jaemin Kim, Sangyoung Park, Kitae Kim(Seoul National University), Massoud Pedram (University of Southern California) and Naehyuck Chang (SNU)	
	An Embedded Flash Memory in a Generic 65nm Logic Process for Zero-Standby-Power System-on-Chip Applications Seung-Hwan Song, Ki Chul Chun and Chris H. Kim (University of Minnesota)	
17:30	**Industry Reception**	

Time	Bay Room	Redondo Room
19:00	**Social Event - Banquet**	

Wednesday, August 1, 2012

Time	Bay Room	Redondo Room
7:30	**Breakfast**	
8:30	**Keynote:** Ultra-Low Power Challenges for the Next Generation ASIC Speaker: Uming Ko, MediaTek USA Chair: Ajith Amerasekera (Texas Instruments)	
9:30	**Break**	
10:00 - 12:00	**Session 13: Processor Design and Implementation** Chair: Lawrence Clark (Arizona State U. and SuVolta, Inc.), Co-Chair: Sujat Jamil (Marvell)	**Session 14: Memory Management and Scheduling** Chair: Naehyuck Chang (Seoul National Univ.), Co-Chair: Guangyu Sun (Peking Univ.)
10:00	*The Core-C6 (CC6) Sleep State of the AMD Bobcat x86 Microprocessor* Aaron Rogers, David Kaplan, Eric Quinnell, Bill Kwan (AMD Austin)	*Reducing L1 Caches Power By Exploiting Software Semantics* Zhen Fang (NVIDIA); Li Zhao, Xiaowei Jiang, Shih-lien Lu, Ravi Iyer, Tong Li (Intel Corp.); Seung Eun Lee (Seoul National University of Science and Technology)
10:30	*Evaluation of Voltage Stacking for Near-Threshold Multicore Computing* Sae Kyu Lee, David Brooks, Gu-Yeon Wei (Harvard University)	*DRAM Power-Aware Rank Scheduling* Sukki Kim (LG Electronics), Soontae Kim, Yebin Lee (Korea Advanced Institute Science and Technology)
11:00	*CHARM: A Composable Heterogeneous Accelerator-Rich Microprocessor* Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Beayna Grigorian, Glenn Reinman (UCLA)	*Energy-Efficient GPU Design with Reconfigurable In-Package Graphics Memory* Jishen Zhao (The Pennsylvania State University); Guangyu Sun (Peking University); Gabriel H. Loh (AMD); Yuan Xie (PSU & AMD)

Time	Bay Room	Redondo Room
11:30	*Something Old and Something New: P-States Can Borrow Microarchitecture Techniques Too* Yasuko Eckert (AMD & U. of Wisconsin-Madison), Srilatha Manne, Michael J. Schulte (Advanced Micro Devices); David A. Wood (University of Wisconsin-Madison & AMD)	*Fan-Speed-Aware Scheduling of Data Intensive Jobs* Christine S. Chan, Yanqin Jin, Yen-Kuan Wu (University of California, San Diego); Kenny Gross, Kalyan Vaidyanathan (Oracle Physical Sciences Research Center); Tajana Šimunić Rosing (UCSD)
		Procedure Hopping: a Low Overhead Solution to Mitigate Variability in Shared-L1 Processor Clusters Abbas Rahimi (University of California, San Diego); Luca Benini (Università di Bologna); Rajesh Gupta (UCSD)