Challenges in Low-Power Analog Circuit Design for sub-28nm CMOS Technologies

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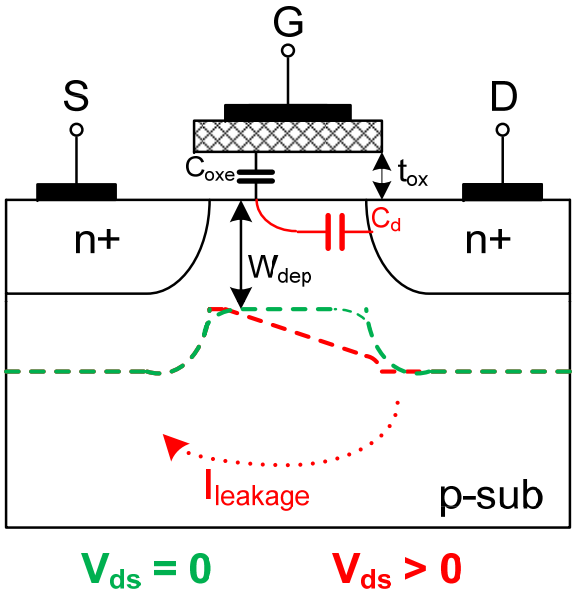
International Symposium on Low Power Electronics and Design

Outline

- Scaling Effects
- Design Methodology
- Challenges in sub-28nm CMOS
- Analog Design for sub-28nm CMOS
- Design Examples
- Conclusions

Scaling Effects

- **Transistor cross section:**



$$V_s = \frac{C_{ox} \cdot V_g + C_d \cdot V_d}{C_{ox}\left(1 + \frac{C_d}{C_{ox}}\right) + C_{dep}} \quad \rightarrow \; V_s \propto V_d$$

$$V_b = \frac{C_{oxe} \cdot V_g + C_d \cdot V_d}{C_{oxe}\left(1 + \frac{C_d}{C_{ox}}\right) + C_{dep}}$$

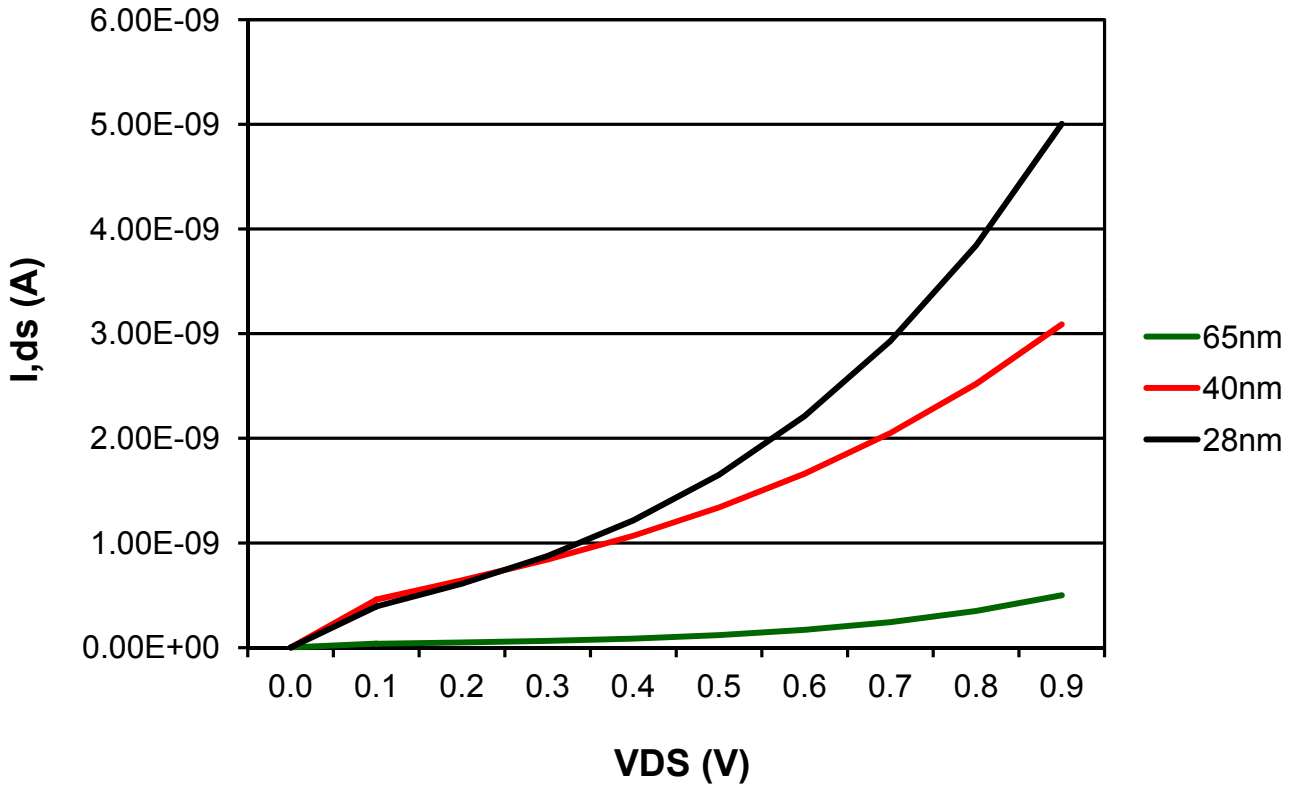
→ $I_{leakage}$ more in deep substrate

Where: $C_{oxe} = \frac{C_{ox} \cdot C_{dep1}}{C_{ox} + C_{dep1}}$

- **Known as *drain induced barrier lowering* (DIBL)**
- **As L scales: 1) Cox↑ 2) W_{dep} ↓(body doping)**

Scaling Effects

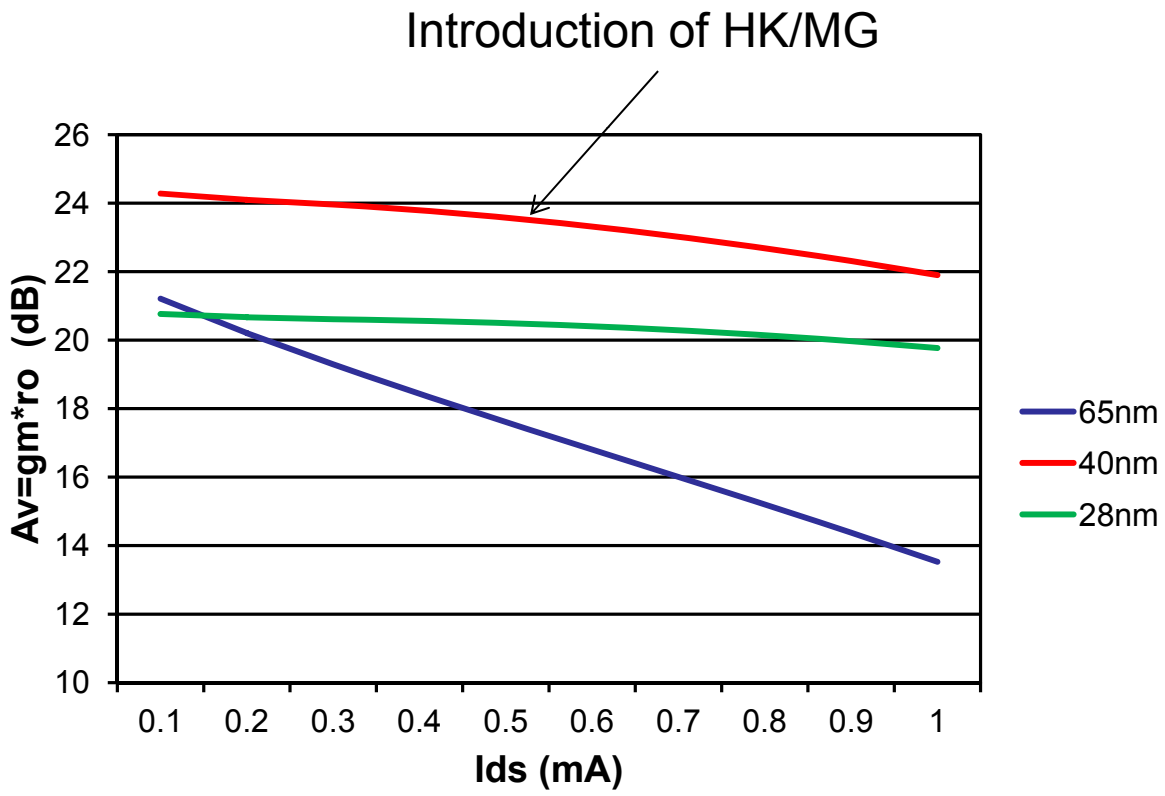
- **Leakage current scaling (W=1um)**

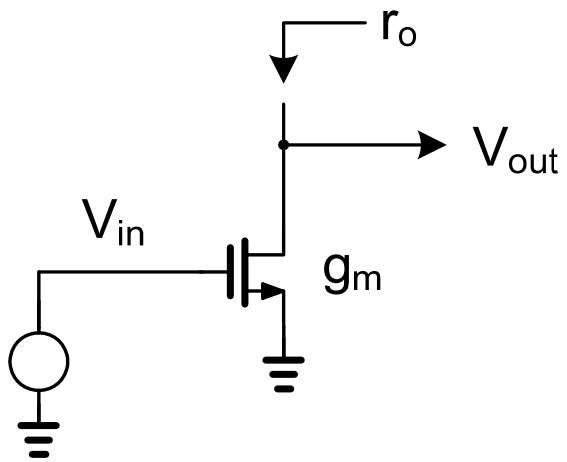


$$I_D = I_{S0} W e^{\frac{q}{KT}(AV_{GS} + BV_{DS})}$$

Scaling Effects

- **Intrinsic Transistor Gain: $A_v = g_m \cdot r_o$**





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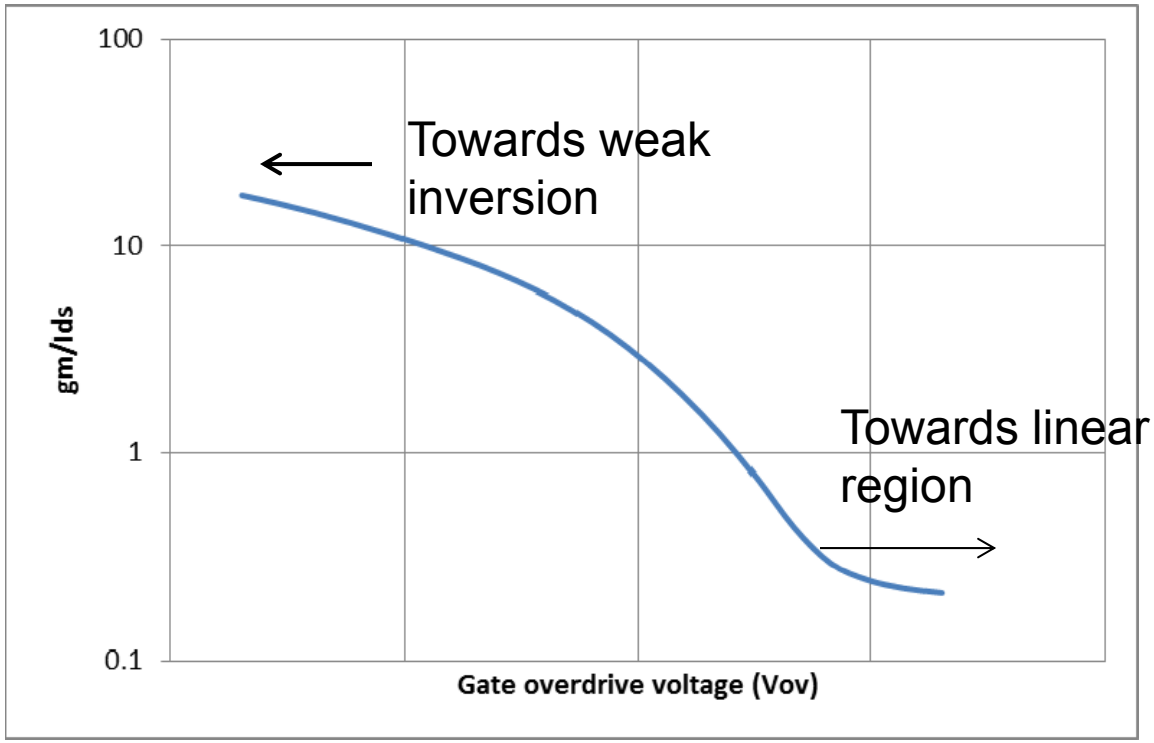
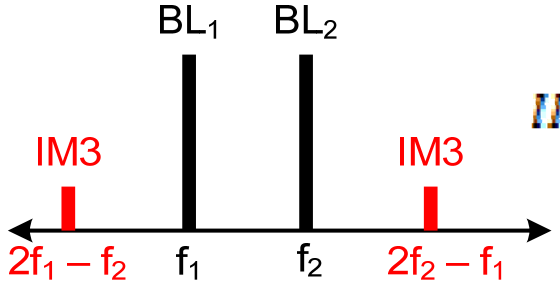
Design Methodology

- **Important Figure-of-merit in analog design is the G_m/I_{DS} ratio**



Design Methodology

- **Other important metrics in analog design include:**
  - **<u>Noise</u>: limits the minimum detectable signal (MDS) that the analog circuit can process**
  - **<u>Linearity</u>: limits the maximum possible signal that the analog circuit can process**



$$IIP3(dBm) = P_{BL}(dBm) + \frac{P_{BL}(dBm) - P_{IM3}(dBm)}{2}$$

  - **Noise+Linearity → define the "dynamic range" (DR) of the signal that the circuit can handle**

$$DR = \frac{2}{3}\left(IIP3 - MDS\right)$$

Design Methodology

- **Other important metrics in analog design include:**
  - **Gain (g_m), Bandwidth (F_t), power consumption**

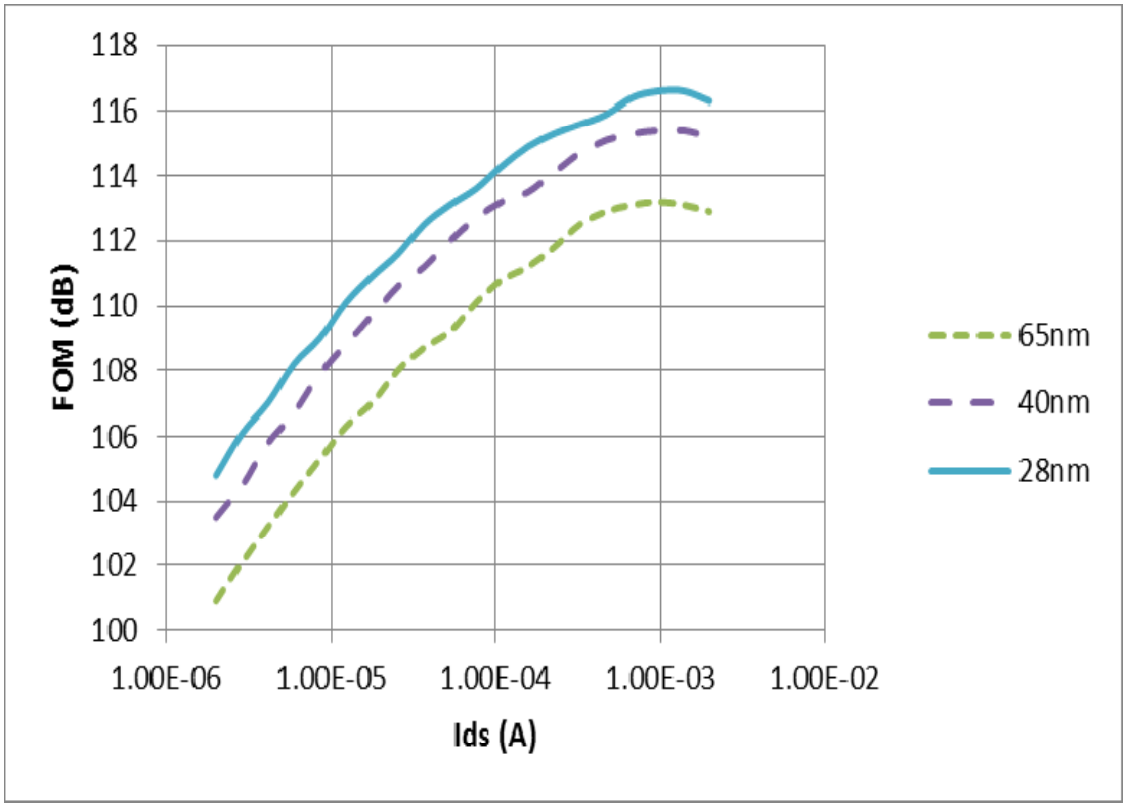
- **Define a "figure-of-merit" (FOM) to take into account dynamic range and bandwidth**
  - **This FOM describes maximum performance without regard to power consumption**

$$FOM = 10\log(f_T) + \frac{2}{3}\left(IIP3 - 10\log\left(\int v_n^2 df\right)\right)$$

Bandwidth **Dynamic range**

Design Methodology

- **FOM plot over current consumption:**



$$FOM = 10\log(f_T) + \frac{2}{3}\left(IIP3 - 10\log\left(\int v_n^2 df\right)\right)$$

Design Methodology

- **Define another "figure-of-merit" (FOM2) to take into account current consumption as well**
  - **FOM2 takes into account the current efficiency in obtaining a certain performance level**

$$FOM2 = 10\log\left(\frac{g_m}{I_{ds}}\right) + 10\log(f_T) + \frac{2}{3}\left(IIP3 - 10\log\left(\int v_n^2 df\right)\right)$$

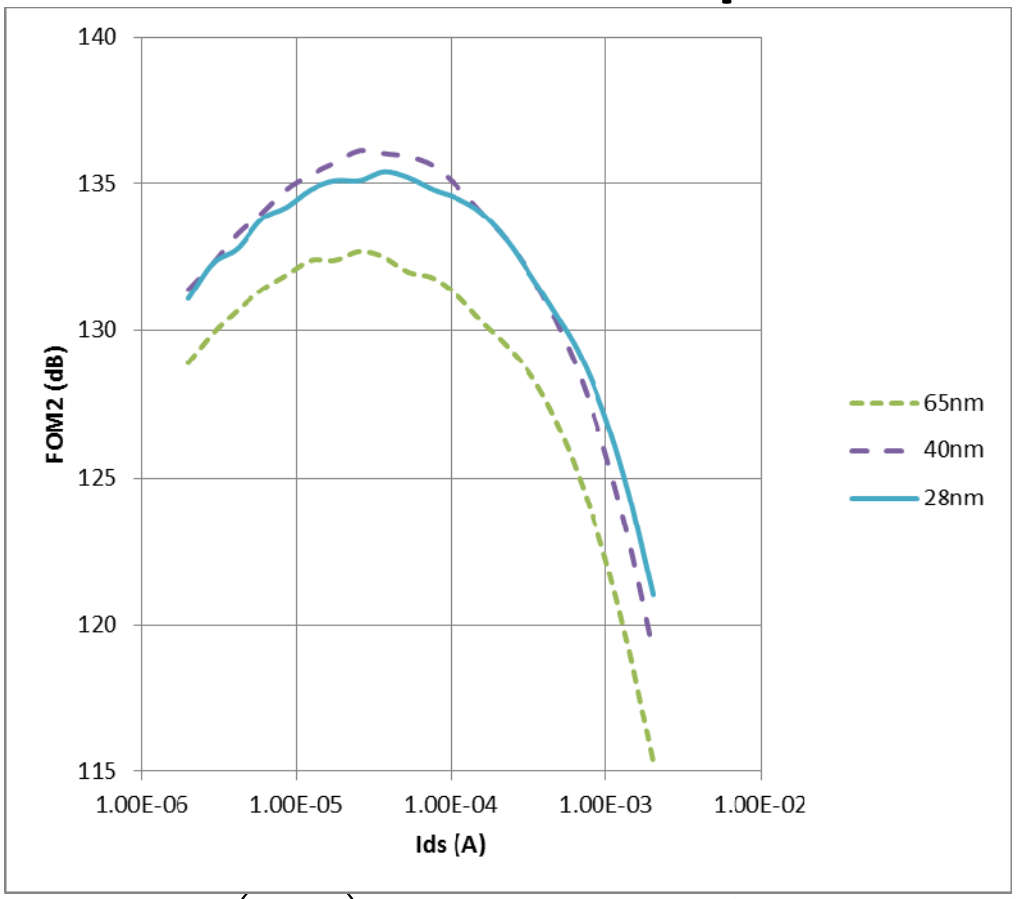
Power Efficiency

Bandwidth

Dynamic Range

Design Methodology

- **FOM2 plot over current consumption**



$$FOM\,2 = 10\log\left(\frac{g_m}{I_{ds}}\right) + 10\log(f_T) + \frac{2}{3}\left(IIP3 - 10\log\left(\int v_n^2 df\right)\right)$$

Design Methodology

- **Overall design methodology:**
  1. **Generate parametric curves based on FOM or FOM2 (Ids and W are parameters)**
  2. **Choose Ids and W that meet desired specifications**

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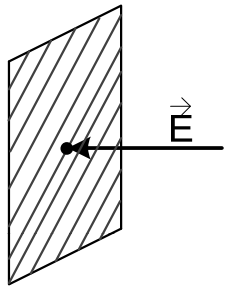
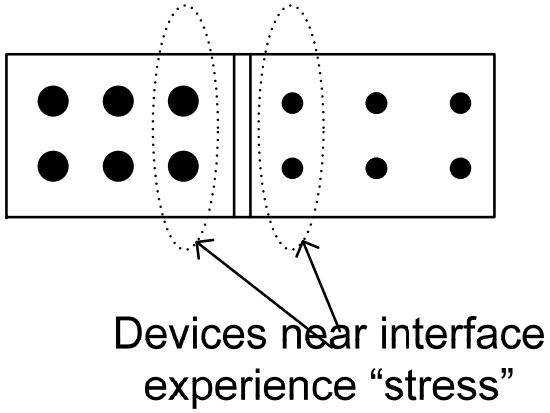
Challenges in sub-28nm CMOS

- **Stress effects (isolation proximity):**
  - **Stress = Force / Area**
  - **Stress scenarios:**
    1. **Force = q * E**

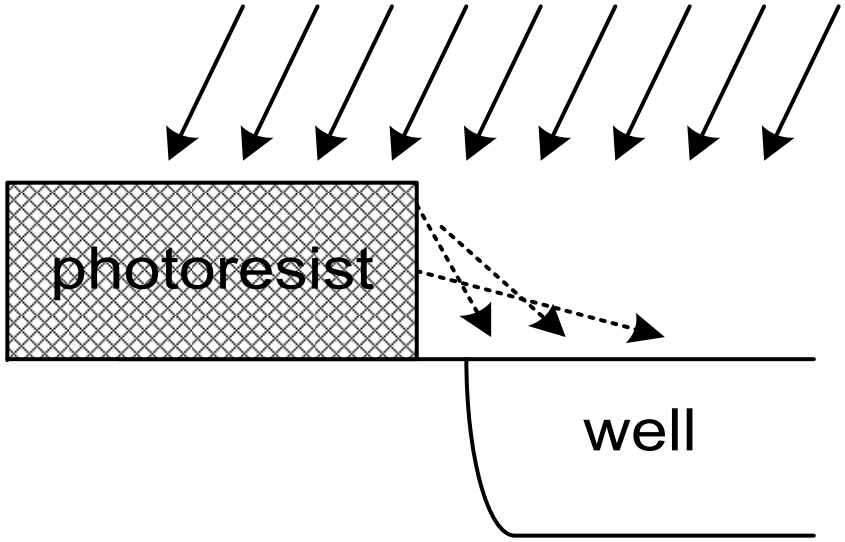




    2. **Stress is also induced by interface boundaries between material with different dopant densities (adjacent NFETs or NFET/PFET boundary)**
  - **Effect of stress → carrier mobility shifts (current!)**
  - **Mitigate by use of dummies & equally spaced devices**

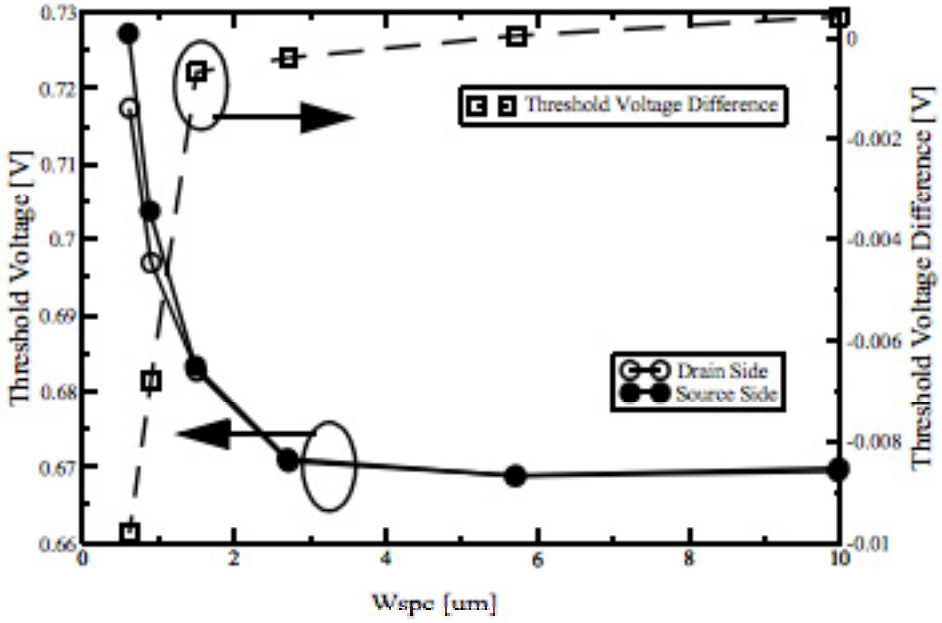
Challenges in sub-28nm CMOS

- **Diffusion proximity (well proximity)**
  - **Dopant atoms scattered from adjacent photoresist**



Scattering → variability in doping profile

VT variation in order to 10's mV

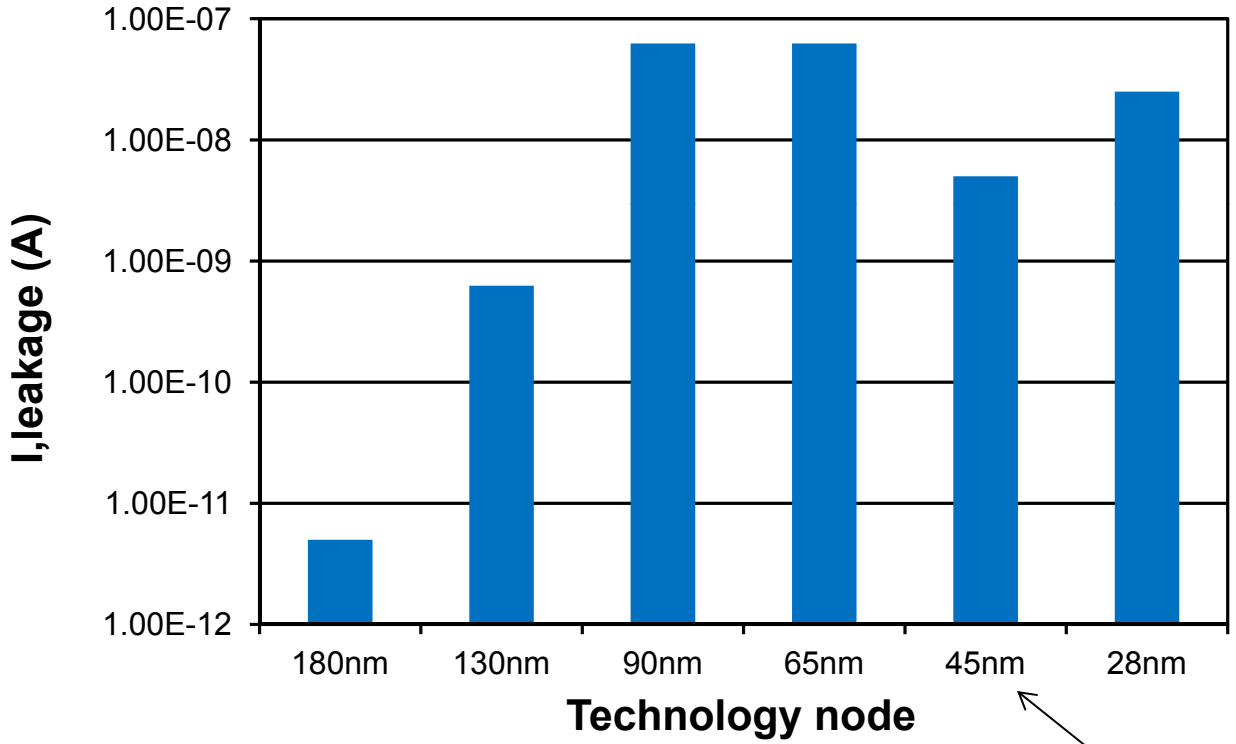


- Mitigate by use of dummies

Source: Freescale Semiconductor (0.13um 3.3V NFET)

Challenges in sub-28nm CMOS

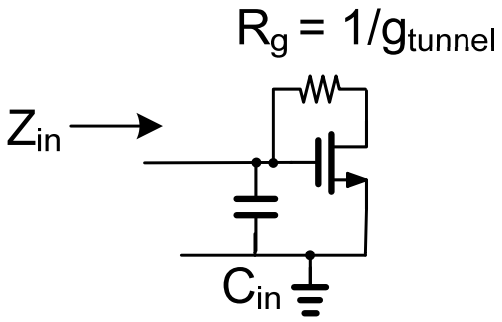
- **Device gate leakage:**
  - **Gate leakage caused by quantum tunneling effect**



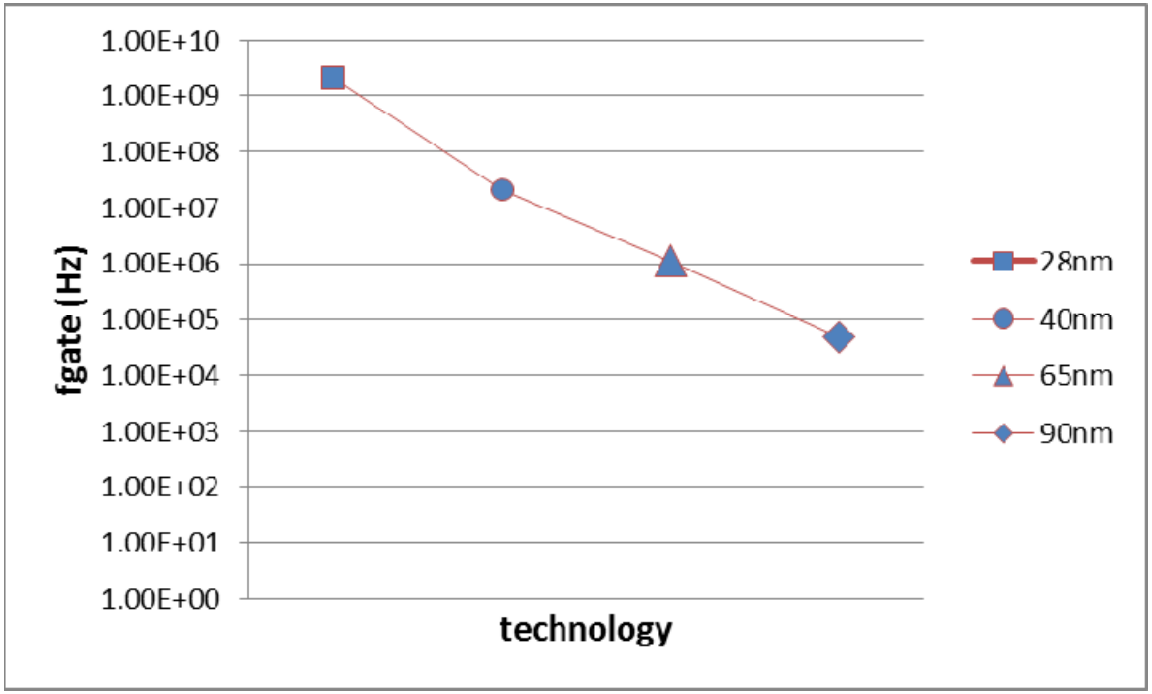
$$i_{GS} \approx C_{ox} \cdot W \cdot L \cdot f_{gate}$$

Challenges in sub-28nm CMOS

- **Gate leakage introduce low-frequency pole:**



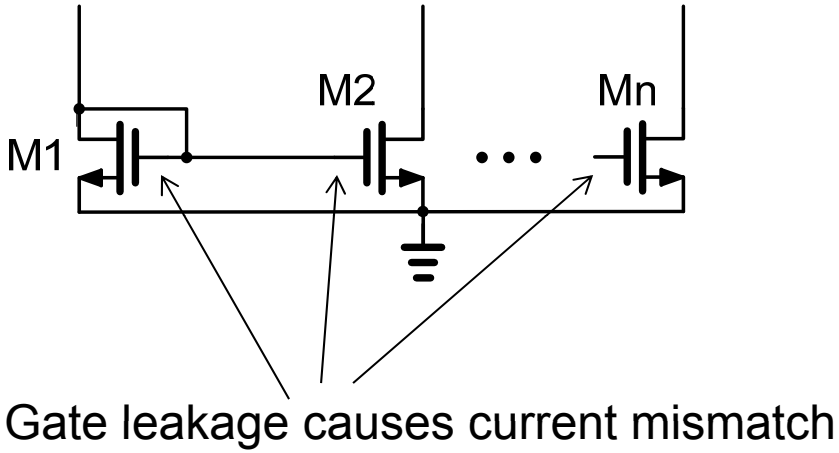
$$f_{gate} = \frac{g_{tunnel}}{2\pi C_{in}}$$



- **This creates a low-frequency bound on sample-and-hold (S/H) circuits as well as low-frequency RC filters (such as PLL loop filters)**

Challenges in sub-28nm CMOS

- **Gate leakage causes mismatch in current mirrors:**



Classical mismatch:

$$\left(\frac{\Delta I}{I}\right)^2 = \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I}\right)^2$$

Mismatch with gate tunneling:

$$\left(\frac{\Delta I}{I}\right)^2 = \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I}\right)^2 + \left(\frac{X_{IGS}}{\sqrt{WL}} \cdot \frac{i_G}{I}\right)^2$$

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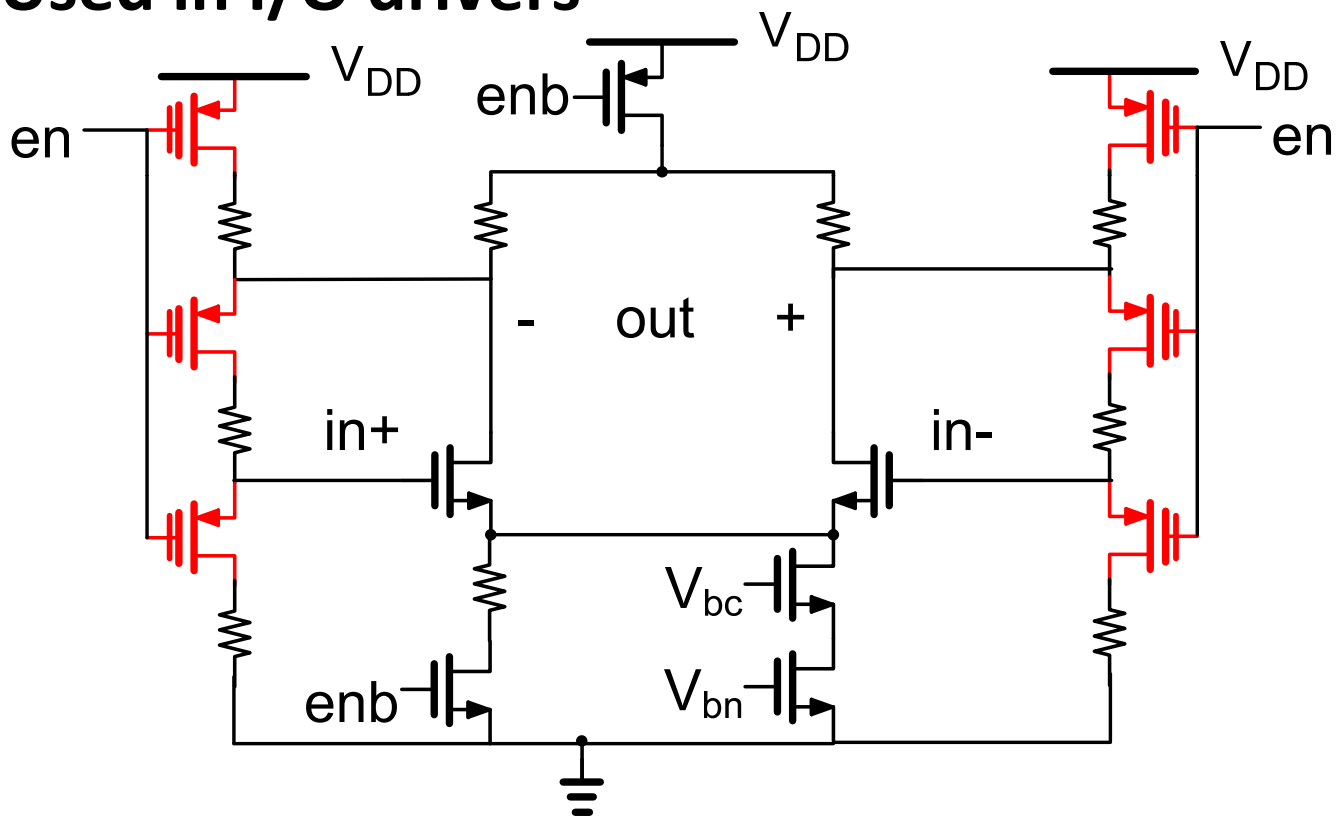
Sub-28nm CMOS Circuit Design

- **Stack devices**
  - **Ensure no stressed oxides during off mode**
  - **Used in I/O drivers**

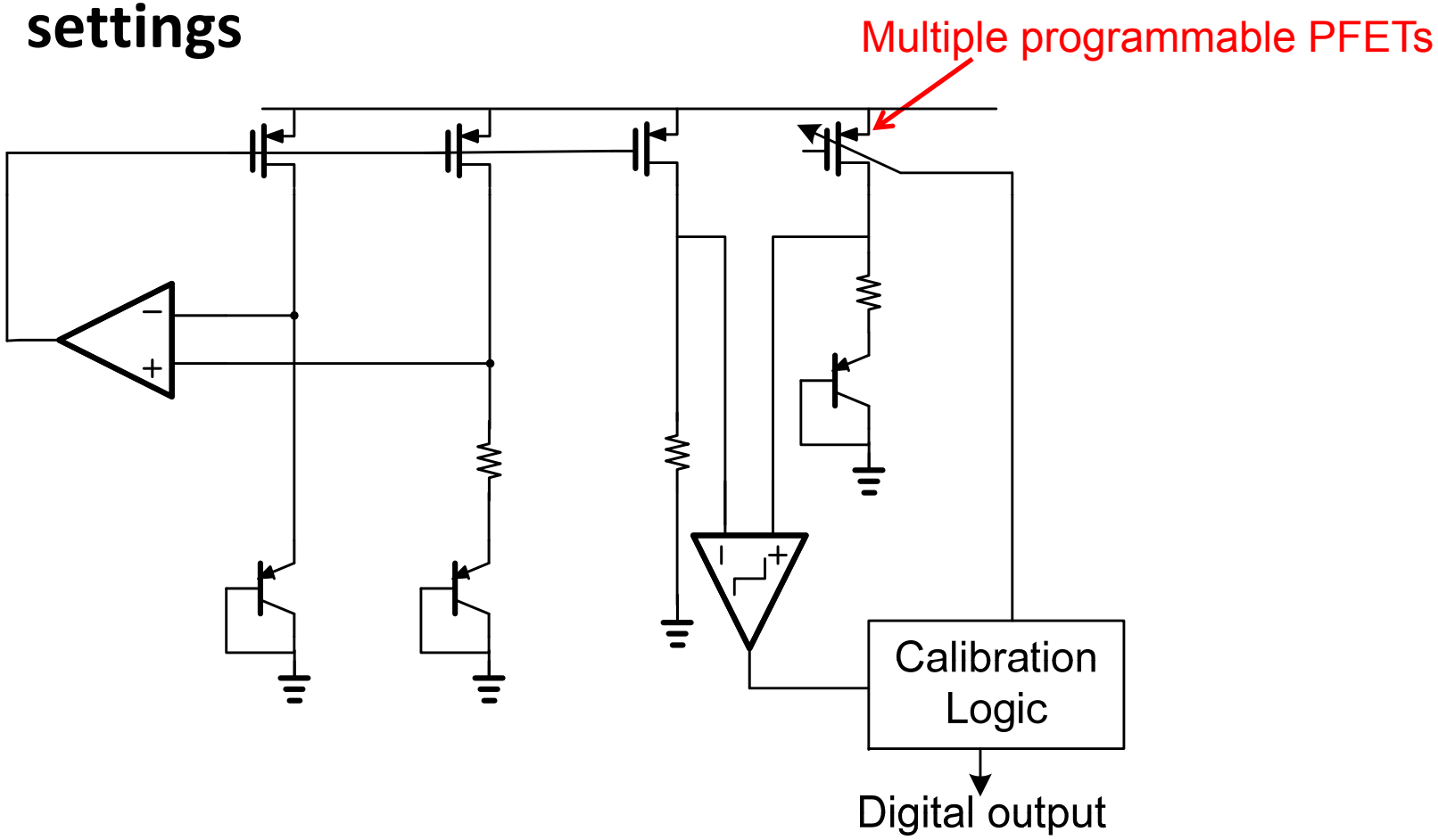


Sub-28nm CMOS Circuit Design

- **Digitally assisted analog circuit design**
  - **Use trimming/calibration loops to sense imperfections in analog circuits → mismatches, center frequency, etc.**
  - **Data converters (DAC/ADC):**
    - **Use a higher resolution, lower frequency ADC/DAC to sense imperfections**
    - **Input voltage (or digital word) is a saw-tooth waveform during calibration**
  - **VCO:**
    - **Trim center frequency**
    - **Trim LC tank amplitude**

Sub-28nm CMOS Circuit Design

- **Design techniques:**
  - **Digital temperature sensor → use to adjust analog settings**



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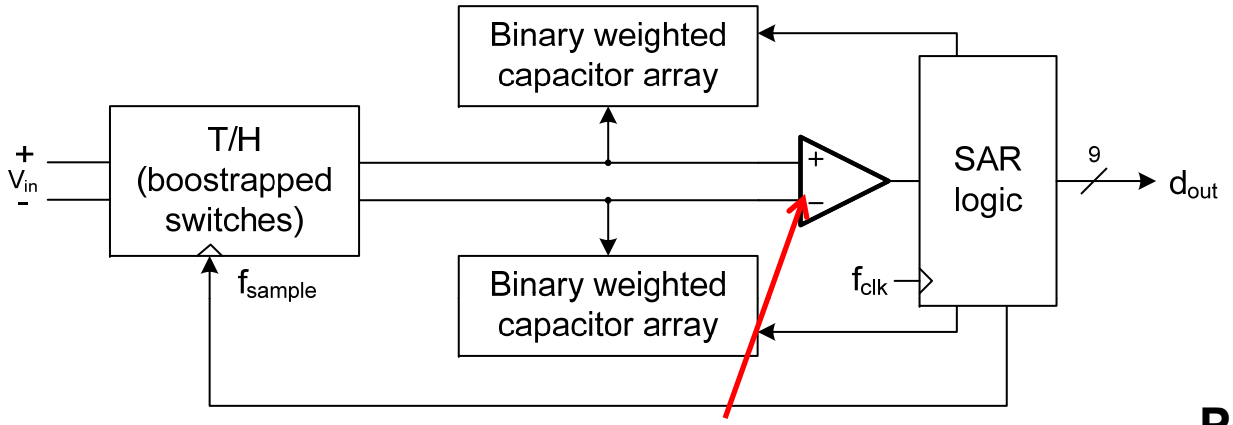
Design Examples

- **9-bit SAR ADC in 28nm CMOS**



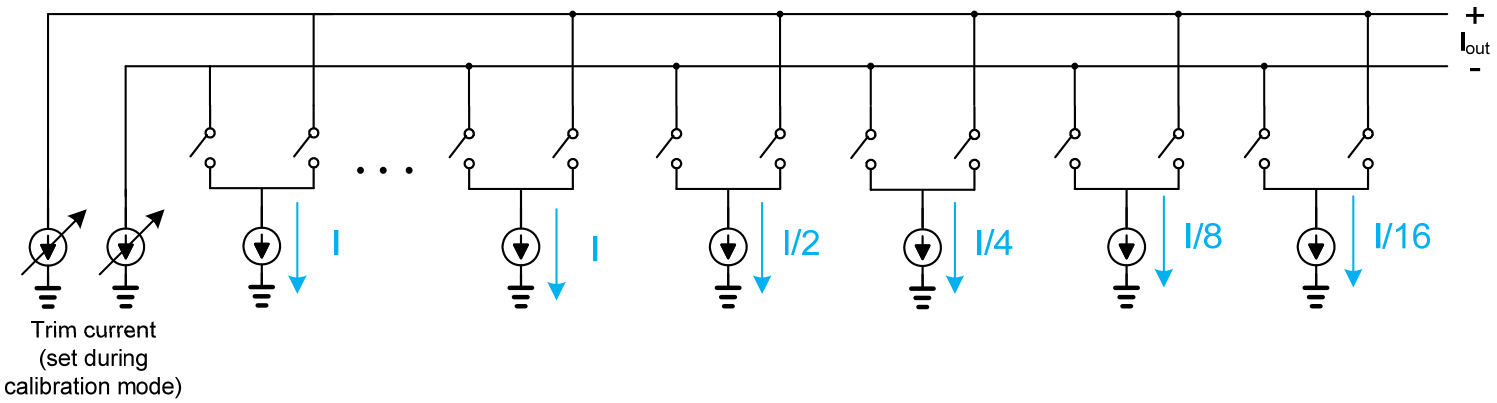
Input offset voltage calibrated at startup (DC calibration loop)

Performance Summary:

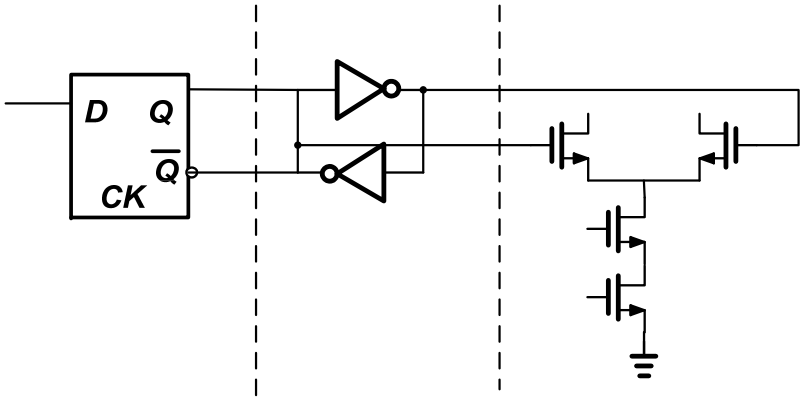
Metric	Value
# bits	9
V_{DD}	0.9
f_{CLK}	900MHz
Area	200um x 100um
Power	382uW
ENOB	8.51

Design Examples

- **10-bit current steering DAC in 28nm CMOS**



- **One Slice:**

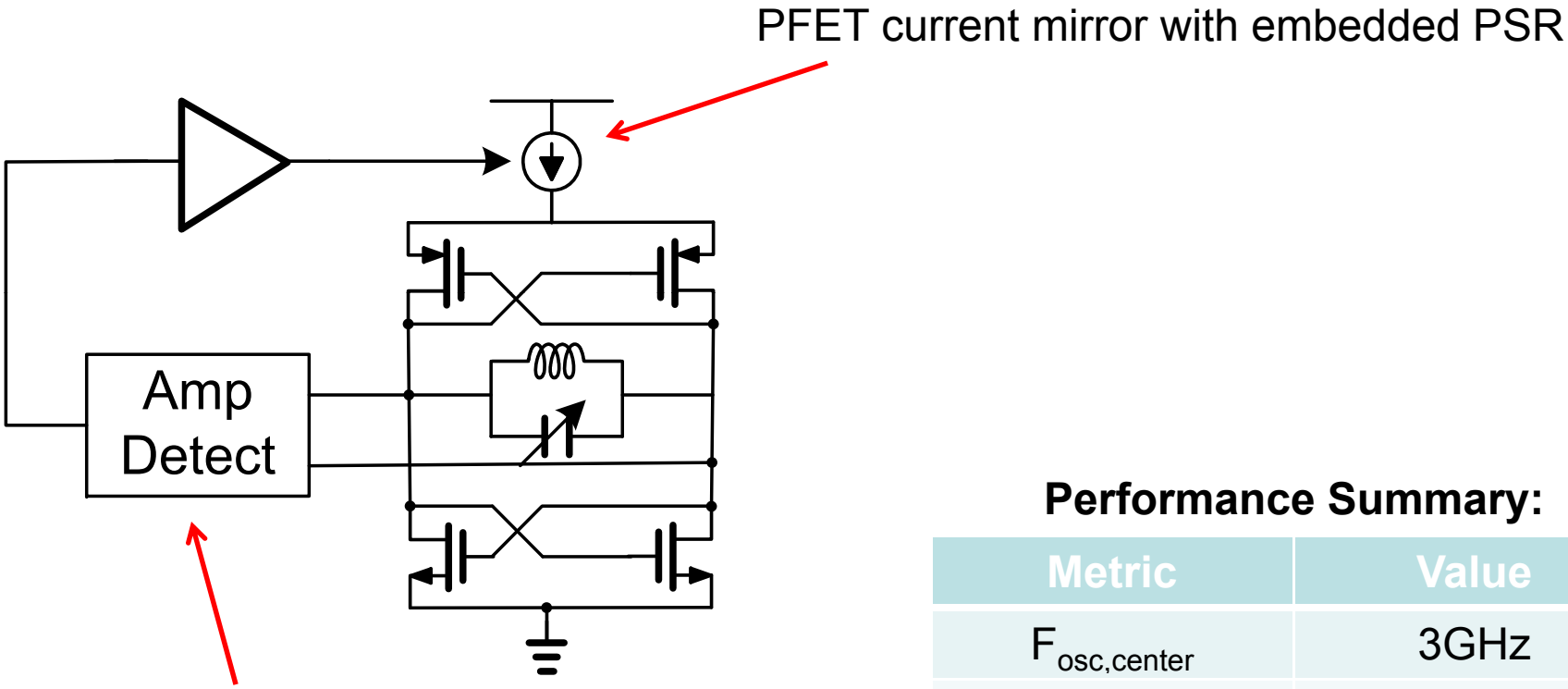


Performance Summary:

Metric	Value
# bits	10
V_{DD}	0.9
f_{CLK}	200MHz
Area	200um x 100um
Power	330uA
ENOB	8.8 bits

Design Examples

- **VCO in 28nm CMOS:**



Performance Summary:

Metric	Value
$F_{osc,center}$	3GHz
Tuning range	800MHz
PN @ 1MHz	-134.3dBc/Hz
Power	9mA

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Conclusions

- Scaling Effects Reviewed
- Design Methodology
  - Based on gm/ID design methodology
  - Extended to include DR & BW

Conclusions

- **Challenges in sub-28nm CMOS analog design**

DSM effect	Analog Circuit Implication
Stress effects (isolation proximity)	Mobility variation (BW, current mismatch, gain)
Diffusion proximity	VT variation (mismatch)
Gate leakage	Noise, mismatch, low-frequency limit

- **Analog circuit design techniques**

Design Technique	Reason / Application
FET stacking	High voltage swing
Digital assist / temp sensor	Trimming analog

- **Design examples: DAC, ADC, VCO**