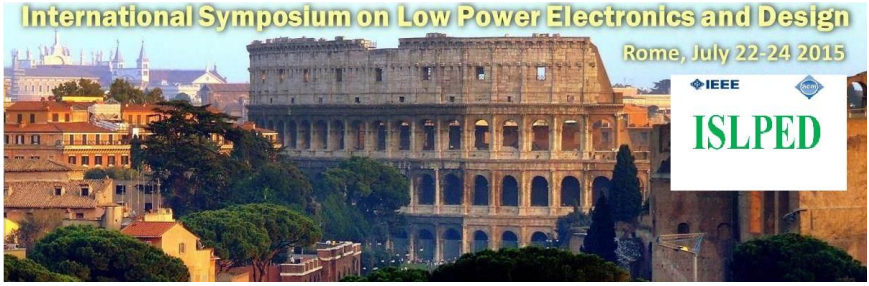

2015 Conference Program

Cloister of San Pietro in Vincoli,
Rome, Italy

Message from the General Chairs

On behalf of the Organizing Committee, it is our pleasure to welcome you to the 20th IEEE/ACM International Symposium on Low Power Electronics and Design, 2015, (ISLPED'15), held in Rome, Italy, on July 22-24, 2015. 20 years ago, a group of visionaries noted the avid interest in low-power design in many different disciplines and recognized the need to bring these diverse groups together with the goal of information sharing, and ISLPED was born. In this year's program, we mark the 20th anniversary of this conference with special awards, a new Industry Reception dinner, and a Founders' Panel.

ISLPED'15 is hosted by Sapienza University of Rome at the Cloister of San Pietro in Vincoli (Saint Peter in Chains), a five-century-old building in the middle of the historical center of the "eternal city", at walking distance from the Colosseum. The 2700-year history of Rome has made the city a unique place in the world for richness of artistic, cultural, historical, and religious treasures. Yet, Rome is also a modern city where more than 3 million people work every day in almost all fields of commerce and industry. Sapienza University of Rome is one of the three public universities in the city and is the largest university in Europe in terms of number of students.

ISLPED (Web: www.islped.org, Twitter: @islped) continues to be the premier forum for the presentation of latest advances in all aspects of low-power design and technologies, ranging from process and circuit technologies, simulation and synthesis tools, to system-level design and software optimization. This year we continue the tradition of gathering top-level contributions from the low-power design community, with renewed emphasis on relations with industry. The Technical Program, led by Co-Chairs Vijay Raghunathan (Purdue University) and Ruchir Puri (IBM), includes a new "Industry Perspective" track with dedicated Co- Chairs Edith Beigne (CEA-LETI) and Jurgen Karmann (Infineon). Many thanks to the Technical Program Committee composed of leading researchers in low-power design, who have generously volunteered their time for the review process of the submitted articles. Following the ISLPED tradition, the conference includes the Low Power Design Contest, chaired by Alberto Macii (Politecnico di Torino) and Hiroki Matsutani (Keio University), where students can showcase hands-on-designs targeted to solve practical problems.

Industry Liaison Co-Chairs, John Biggs (ARM) and David Garrett (Broadcom), have done an outstanding job in raising strong industry support. This year, ISLPED sponsoring team has reached the outstanding number of 9 industrial sponsors among the world's most representative companies in electronics and CAD: ARM, Intel, MunEDA, and Synopsys (Gold Sponsors); IBM, Cadence, Micron, NanoTera, and NXP (Silver sponsors); and the 2 academic sponsors Sapienza University of Rome (Gold) and University of Bologna (Silver).

The ISLPED'15 Organizing Committee has been working hard to offer you a top-class conference experience. Alessandro Trifiletti, Local Arrangement Chair, has prepared this year's very special venue and the dinner events. We thank Yu Wang for serving as Treasurer, Theo Theocharides as Web Chair, Deming Chen, Baris Taskin, and Andreas Burg as Publicity Co-Chairs, Paul Wesling as Publication Chair, and finally the Local Staff team who helped in many ways. We are also grateful to the Executive Committee, chaired by Massoud Pedram (USC), for their guidance.

ISLPED'15 is co-sponsored by IEEE-CAS and ACM-SIGDA, with technical support from the IEEE-SSCS, from Sapienza Univ. Digital Circuits and Systems Group, and from EvoElectronics.

We truly hope that you enjoy the excellent ISLPED'15 program and have a pleasant, fascinating and unique experience in Rome.

Luca Benini
Univ. of Bologna, Italy;
ETH Zurich, Switzerland.

Renu Mehra
Synopsys,
San Francisco, CA

Mauro Olivieri
Sapienza University of Rome, Italy.

Message from the Program Chairs

It is our great pleasure to welcome you to the 2015 ACM/IEEE International Symposium on Low Power Electronics and Design – ISLPED'15, in the "eternal city" of Rome, Italy. This year's symposium continues its two decade long tradition of being the premier forum for presentation of research results and industrial experience reports on leading-edge issues in low power design. ISLPED has always been unique in the sense that it brings together researchers and practitioners interested in various aspects of low power design at a single venue and provides them an opportunity to share their perspectives with each other.

This year, the call for papers attracted 198 submissions from Asia, Africa, Europe, and North & South America, including several submissions to the new "Industrial Perspectives" track that was introduced this year. Of these, the Technical Program Committee (TPC) accepted a total of 61 papers with 39 full-length presentations and 22 poster presentations. The accepted papers cover a variety of low-power topics in technologies, circuits, logic & architecture, CAD tools & methodologies, systems & platforms, and software & applications.

In addition to the research papers, this year's technical program also features:

- Three exciting Keynote Speeches by Prof. Alberto Sangiovanni-Vincentelli from the University of California, Berkeley, Dr. Jose Pineda de Gyvez from NXP Semiconductors, and Prof. Naresh Shanbhag from the University of Illinois, Urbana Champaign.
- Four Invited Plenary Talks on a variety of emerging low-power topics, ranging from implantable medical devices to power management in server-class processors.
- An evening founders' panel to mark the 20th anniversary of ISLPED and reflect on the road ahead.
- Winning entries from the low power design contest, ably conducted by our design contest co-chairs.

We hope that the above events will complement our main program by providing you with a broader perspective of state-of-the-art in low power design as well as give you valuable insights into future trends.

Putting together a rich and strong technical program would not have been possible without the help of a large number of people. We are thankful to all the authors for a stellar set of submissions. We are indebted to our outstanding TPC members, who worked for weeks reviewing and selecting the papers that appear in the program, and providing constructive and careful feedback to authors. Our many thanks go to the ISLPED 2015 organizing committee, led by the general co-chairs, who made everything work like clockwork. Finally, thanks to the attendees of ISLPED 2015 for your continued patronage and participation, which is what makes our conference such a fertile venue for the exchange of cutting-edge ideas in low power design.

We hope you have a very enjoyable and intellectually stimulating ISLPED 2015 and also find some time to soak in the unforgettable sights of this ancient, beautiful, and unique city!

Ruchir Puri
IBM Research, USA

Vijay Raghunathan
Purdue University, USA

Program at a Glance: Wednesday, July 22

8:00-8:30	Conference Registration	
8:30-9:00	Welcome Address: Room 1	
9:00-10:00	Keynote 1: Room 1	
	Let's Get Physical: Adding Physical Dimensions to Cyber Systems *Alberto Sangiovanni-Vincentelli, University of California, Berkeley*	
10:00-10:30	Coffee Break: Cloister	
10:30-12:30	Session 1: Room 1	Session 2: Cloister Room
	Emerging Technologies for Energy Efficiency	Thermal Management and Cooling
12:30-1:30	Lunch: Cloister	
1:30-3:00	Invited Plenary Session: Room 1	
3:00-4:00	Coffee Break with Posters: Cloister	
4:00-6:00	Session 3: Room 1	Session 4: Cloister Room
	Low Power Memory Organization	Approximate Computing and Neuromorphic Architectures
6:30 -	Industry Cocktail Reception, followed by Awards Ceremony (starting at 7pm), and Industry Reception Dinner (Cloister)	

Program at a Glance: Thursday, July 23

8:30-9:30	Keynote 2: Room 1	
	Opportunities in System Power Management for High Performance Mixed Signal Platforms *Jose Pineda de Gyvez, NXP Semiconductors*	
9:30-10:00	Coffee Break: Cloister	
10:00-12:00	Session 5: Room 1	Session 6: Cloister Room
	Energy Efficient On-Chip Communication	Low Power Techniques for Robust and Secure Design; Design Contest Winners
12:00-1:30	Lunch: Cloister	

1:30-3:00	Invited Plenary Session: Room 1	
3:00-3:30	Coffee Break: Cloister	
3:30-5:30	Session 7: Room 1	Session 8: Cloister Room
	Optimizing Power Supply and Delivery	Low Power Software and Systems
5:45-7:00	Special Evening Panel: Room 1	
	"20 Years of ISLPED – Past, Present, and Future"	
7:30 -	2015 ISLPED Banquet and Dinner	

Program at a Glance: Friday, July 24

8:30 - 9:30	Keynote 3: Room 1	
	Statistical Information Processing: Computing for the Nanoscale Era *Naresh Shanbhag, University of Illinois at Urbana Champaign*	
9:30-10:15	Coffee Break with Posters: Cloister	
10:15-12:15	Session 9: Room 1	Session 10: Cloister Room
	Efficient Power Modeling, Estimation, and Optimization	Dynamic Adaptation Techniques for Energy Efficiency

Detailed Program: Wednesday, July 22

8:00 - 8:30	**Conference Registration**	
8:30 - 9:00	**Welcome by General Co-Chairs and Technical Program Co-Chairs and presentation of the IEEE CASS C.A. Desoer Technical Achievement Award (Room 1)**	
9:00 - 10:00	**Keynote 1: "Let's Get Physical: Adding Physical Dimensions to Cyber Systems,"** *Alberto Sangiovanni-Vincentelli, University of California, Berkeley* **(Room 1)** *Session Chair: Luca Benini, ETH Zurich and University of Bologna*	
10:00 - 10:30	**Coffee Break (Cloister)**	
10:30 - 12:30	**Session 1: Emerging Technologies for Energy Efficiency (Room 1)** *Session Chair: Saibal Mukhopadhyay, Georgia Tech.*	**Session 2: Thermal Management and Cooling (Cloister Room)** *Session Chair: Jiang Hu, Texas A&M University*
	1.1. COAST: Correlated Material Assisted STT MRAMs for Optimized Read Operation *Ahmedullah Aziz, Nikhil Shukla, Suman Datta, and Sumeet Gupta* *Pennsylvania State University* **1.2.** A Novel Slope Detection Technique for Robust STTRAM Sensing *Seyedhamidreza Motaman[1], Swaroop Ghosh[1], and Jaydeep Kulkarni[2]* *[1]University of South Florida, [2]Intel* **1.3.** Optimizing Boolean Embedding Matrix for Compressive Sensing in RRAM Crossbar *Yuhao Wang[1], Xin Li[1], Hao Yu[1], Leibin Ni[1], Wei Yang[2], Chuliang Weng[2], and Junfeng Zhao[2]* *[1]Nanyang Technological University, [2]Huawei Technologies Co., Ltd* **1.4.** Fine-Grained Write Scheduling for PCM Performance Improvement under Write Power Budget	**2.1.** A Simulation Framework for Rapid Prototyping and Evaluation of Thermal Mitigation Techniques in Many-Core Architectures **(Industry Perspectives)** *Tanguy Sassolas[1], Chiara Sandionigi[2], Alexandre Guerre[1], Julien Mottin[3], Pascal Vivet[3], Hela Boussetta[4], and Nicolas Peltier[4]* *[1]CEA LIST, [2]CEA, [3]CEA LETI, [4]Docea Power* **2.2.** Making Sense of Thermoelectrics for Processor Thermal Management and Energy Harvesting *Sriram Jayakumar and Sherief Reda* *Brown University* **2.3.** Adaptive Sprinting: How to Get the Most Out of Phase Change Based Passive Cooling *Fulya Kaplan and Ayse Coskun* *Boston University* **2.4.** Experimental Characterization

	Chun-Hao Lai[1], Shun-Chih Yu[1], Chia-Lin Yang[1], and Hsiang-Pang Li[2] *[1]National Taiwan University, [2]MXIC Corp*	of In-Package Microfluidic Cooling on a System-On-Chip (Best Paper Nominee) *Wen Yueh, Zhimin Wan, Yogendra Joshi, Saibal Mukhopadhyay* *Georgia Institute of Technology*
12:30 - 1:30	**Lunch (Cloister)**	
1:30 - 3:00	**Invited Plenary Talks (Room 1)** *Session Chair: Vijay Raghunathan (Purdue University)*	
	I-1. Power Management in the Intel Xeon E5 v3 *Ankush Varma, Bill Bowhill, Jason Crop, Corey Gough, Brian Griffith, Dan Kingsley, and Krishna Sistla, Intel Inc.* **I-2.** Resonant Clock Designs on the IBM POWER8 and z13 Processors from 2 to 5 GHz *Phillip Restle, IBM Research*	
3:00 - 4:00	**Coffee Break with Posters (Cloister)**	
4:00 - 6:00	**Session 3: Low Power Memory Organization (Room 1)** *Session Chair: David Garrett, Broadcom Inc.*	**Session 4: Approximate Computing and Neuromorphic Architectures (Cloister Room)** *Session Chair: Francesca Palumbo, University of Sassari*
	3.1. Reducing Dynamic Energy of Set-Associative L1 Instruction Cache by Early Tag Lookup (Best Paper Nominee) *Wei Zhang, Hang Zhang, and John Lach* *University of Virginia* **3.2.** Bank Stealing For Conflict Mitigation in GPGPU Register File *Naifeng Jing, Shuang Chen, Shunning Jiang, Li Jiang, Chao Li, and Xiaoyao Liang* *Shanghai Jiao Tong University* **3.3.** Leveraging Emerging Nonvolatile Memory in High-Level Synthesis with Loop Transformations *Shuangchen Li[1], Ang Li[2], Yuan Zhe[2], Yongpan Liu[2], Peng Li[3], Guangyu Sun[4],*	**4.1.** Design of Fine-grained Sequential Approximate Circuits using Probability-aware Fault Emulation *David May and Walter Stechele* *Technische Universität München* **4.2.** Hybrid Approximate Multiplier Architectures for Improved Power-Accuracy Trade-offs *Georgios Zervakis, Sotirios Xydis, Kostas Tsoumanis, Dimitrios Soudris, and Kiamal Pekmestzi* *National Technical University of Athens (NTUA)* **4.3.** A Power-Aware Digital Feedforward Neural Network Platform with Backpropagation

	Yu Wang[2], Huazhong Yang[2], and Yuan Xie[1] *[1]University of California, Santa Barbara, [2]Tsinghua University, [3]University of California, Los Angeles, [4]Perking University* **3.4.** Enabling Energy Efficient Hybrid Memory Cube Systems with Erasure Codes *Shibo Wang, Yanwei Song, Mahdi Bojnordi, and Engin Ipek* *University of Rochester*	Driven Approximate Synapses *Jaeha Kung, Duckhwan Kim, and Saibal Mukhopadhyay* *Georgia Institute of Technology* **4.4.** A Neuromorphic Neural Spike Clustering Processor for Deep-Brain Sensing and Stimulation Systems *Beinuo Zhang[1], Zhewei Jiang[1], Qi Wang[1], Jae-sun Seo[2], Mingoo Seok[1]* *[1]Columbia University, [2]Arizona State University*
6:30 -	**Industry Cocktail Reception, followed by Awards Ceremony (please note that the awards ceremony will start at 7pm), and Industry Reception Dinner (Cloister)**	

Detailed Program: Thursday, July 23

8:30 - 9:30	**Keynote 2: "Opportunities in System Power Management for High Performance Mixed Signal Platforms,"** *Jose Pineda de Gyvez, NXP Semiconductors* **(Room 1)** *Session Chair: Mauro Olivieri, Sapienza University of Rome*	
9:30 - 10:00	**Coffee Break (Cloister)**	
10:00 - 12:00	**Session 5: Energy Efficient On-Chip Communication (Room 1)** *Session Chair: Chia-Lin Yang, National Taiwan University*	**Session 6: Low Power Techniques for Robust and Secure Design; Design Contest Winners (Cloister Room)** *Session Chair: Andrea Bartolini, ETH Zurich*
	5.1. High-Efficiency Crossbar Switches using Capacitively Coupled Signaling *Cagla Cakir[1], Ron Ho[2], Jon Lexau[3], and Ken Mai[1]* *[1]Carnegie Mellon University, [2]Altera Corp., [3]Oracle Labs* **5.2.** Tackling Voltage Emergencies in NoC Through Timing Error Resilience *Rajesh Jayashankara Shridevi, Dean Michael Ancajas, Koushik Chakraborty,*	**6.1.** Collaborative Gate Implementation Selection and Adaptivity Assignment for Robust Combinational Circuits *Hao He, Jiafan Wang, and Jiang Hu* *Texas A&M University* **6.2.** Analysis of Adaptive Clocking Technique for Resonant Supply Voltage Noise Mitigation (Best Paper Nominee) *Paul Whatmough[1], Shidhartha Das[2], and David Bull[2] [1]Harvard University,*

	and Sanghamitra Roy *Utah State University* **5.3.** An Energy Efficient and Low Cross-talk CMOS Sub-THz I/O with Surface-wave Modulator and Interconnect *Yuan Liang[1], Hao Yu[1], Junfeng Zhao[2], Wei Yang[2], and Yuangang Wang[2]* *[1]Nanyang Technological University,* *[2]Huawei Technologies Co., Ltd.* **5.4.** A Compact Low-Power eDRAM-based NoC Buffer *Cheng Li and Paul Ampadu* *University of Rochester*	*[2]ARM Ltd.* **6.3.** Exploring Power Attack Protection of Resource Constrained Encryption Engines using Integrated Low-Drop-Out Regulators *Arvind Singh, Monodeep Kar, Jong Hwan Ko, and Saibal Mukhopadhyay* *Georgia Institute of Technology* **6.4.** (15 min.) *Design Contest Winner:* A 2.89-uW Clockless Fully-Integrated Wireless ECG SoC for Wearable Sensors Xiaoyang Zhang, Zhe Zhang, Yongfu Li, Changrong Liu, Yong Xin Guo, and Yong Lian National University of Singapore **6.5.** (15 min.) *Design Contest Winner:* Low Power Detection of Sternocleidomastoid Muscle Contraction for Asthma Assessment and Control *Jun Luan and Pai Chou* *University of California, Irvine*
12:00 - 1:30	**Lunch (Cloister)**	
1:30 - 3:00	**Invited Plenary Talks (Room 1)** *Session Chair: Ruchir Puri (IBM Research)* **I-3.** Energy Challenges in Smart Systems Design *Enrico Macii and Massimo Poncino, Politecnico di Torino* *Michelangelo Grosso, ST-POLITO SCARL (STMicroelectronics Group)* **I-4.** Wireless Power Transfer for Implantable Medical Devices *Pedro Irazoqui, Purdue University*	
3:00 - 3:30	**Coffee Break (Cloister)**	
3:30 - 5:30	**Session 7: Optimizing Power Supply and Delivery (Room 1)** *Session Chair: Andrea Calimera, Politecnico di Torino*	**Session 8: Low Power Software and Systems (Cloister Room)** *Session Chair: Davide Brunelli, University of Trento*
	7.1. Fully-Integrated Switched-	**8.1.** Hardware-Software

	Capacitor Voltage Regulator with On-Chip Current-Sensing and Workload Optimization in 32nm SOI CMOS *Xiaoyang Mi[1], Debashis Mandal[1], Visvesh Sathe[2], Bertan Bakkaloglu[1], and Jae-sun Seo[1]* *[1]Arizona State University, [2]University of Washington* **7.2.** Modeling and Characterization of the System-Level Power Delivery Network for a Dual-Core ARM Cortex-A57 Cluster in 28nm CMOS **(Industry Perspectives)** (Best Paper Nominee) *Shidhartha Das, Paul Whatmough, and David Bull* *ARM Ltd.* **7.3.** Transient Voltage Noise in Charge-Recycled Power Delivery Networks for Many-Layer 3D-IC *Runjie Zhang[1], Kaushik Mazumdar[1], Brett Meyer[2], Ke Wang[1], Kevin Skadron[1], and Mircea Stan[1]* *[1]University of Virginia, [2]McGill University* **7.4.** Design and Optimization of a Reconfigurable Power Delivery Network for Large-Area, DVS-Enabled OLED Displays *Woojoo Lee[1], Yanzhi Wang[2], Donghwa Shin[3], Shahin Nazarian[2], and Massoud Pedram[2]* *[1]ETRI, [2]University of Southern California, [3]Yeungnam University*	Interaction for Run-time Power Optimization: A Case Study of Embedded Linux on Multicore Smartphones **(Industry Perspectives)** *Anup Das[1], Matthew Walker[1], Andreas Hansson[1,2], Bashir Al-Hashimi[1], and Geoff Merrett[1]* *[1]University of Southampton, [2]ARM Ltd.* **8.2.** CGSharing: Efficient Content Sharing in GPU-Based Cloud Gaming *Xiangyu Wu, Yuanfang Xia, NaifengJing, and Xiaoyao Liang* *Shanghai Jiao Tong University* **8.3.** Energy Efficient Scheduling for Web Search on Heterogeneous MicroServers *Sankalp Jain[1], Harshad Navale[1], Umit Ogras[1], and Siddharth Garg[2]* *[1]Arizona State University, [2]New York University* **8.4.** Low-Power Detection of Sternocleidomastoid Muscle Contraction for Asthma Assessment and Control *Jun Luan, Seungjae Lee, and Pai Chou* *University of California, Irvine*
5:45-7:00	**Special Evening Panel (Room 1)** **"20 Years of ISLPED – Past, Present, and Future"** **Organizers:** *Naehyuck Chang, Massoud Pedram (moderator), Massimo Poncino, and Mircea Stan* **Panelists:** *Naehyuck Chang, Pai Chou, Vivek De, Enrico Macii, Farid Najm, Vijaykrishnan Narayanan, Wolfgang Nebel, Massimo Poncino, Naresh Shanbhag, Mircea Stan, and Yuan Xie*	

7:30 -	**2015 ISLPED Banquet and Dinner**

Detailed Program: Friday, July 24

8:30 - 9:30	**Keynote 3: "Statistical Information Processing: Computing For The Nanoscale Era,"** *Naresh Shanbhag, University of Illinois at Urbana Champaign* **(Room 1)** *Session Chair: Renu Mehra, Synopsys*	
9:30 - 10:15	**Coffee Break with Posters (Cloister)**	
10:15 - 12:15	**Session 9: Efficient Power Modeling, Estimation, and Optimization (Room 1)** *Session Chair: Massimo Poncino, Politecnico di Torino*	**Session 10: Dynamic Adaptation Techniques for Energy Efficiency (Cloister Room)** *Session Chair: Jose Ayala, University of Madrid*
	9.1. PowerTrain: A Learning-based Calibration of McPAT Power Models *Wooseok Lee[1], Youngchun Kim[1], Jee Ho Ryoo[1], Dam Sunwoo[2], Andreas Gerstlauer[1], and Lizy K. John[1]* *[1]University of Texas at Austin, [2]ARM R&D* **9.2.** FreqLeak: A frequency step based method for efficient leakage power characterization in a system (Best Paper Nominee) *Arun Joseph, Anand Haridass, Charles Lefurgy, Sreekanth Pai, Spandana Rachamalla, and Francesco Campisano* *IBM* **9.3.** Power benefit study of monolithic 3D IC at the 7nm technology node *Kyungwook Chang[1], Kartik Acharya[1], Saurabh Sinha[2], Brian Cline[2], Greg Yeric[2], and Sung Kyu Lim[1]* *[1]Georgia Institute of Technology, [2]ARM Inc.* **9.4.** An Optimal Power Supply And Body Bias Voltage for a Ultra Low Power Micro-Controller with Silicon	**10.1.** Hierarchical Power Budgeting for Dark Silicon Chips *Muhammad Usman Karim Khan, Muhammad Shafique, and Joerg Henkel Karlsruhe Institute of Technology (KIT)* **10.2.** Dynamic Power Management for Many-Core Platforms in the Dark Silicon Era: A Multi-Objective Control Approach *Amir-Mohammad Rahmani[1,2], Mohammad-Hashem Haghbayan[1], Anil Kanduri[1], Awet Yemane Weldezion[2], Pasi Liljeberg[1], Juha Plosila[1], Axel Jantsch[3], and Hannu Tenhunen[1,3]* *[1]University of Turku, [2]KTH Royal Institute of Technology, [3]Vienna University of Technology* **10.3.** DRVS: Power-Efficient Reliability Management through Dynamic Redundancy and Voltage Scaling under Variations *Mohammad Salehi[1], Mohammad Khavari Tavana[2], Semeen Rehman[1], Florian Kriebel[1], Muhammad Shafique[1], Alireza Ejlali[3], and Joerg Henkel[1]* *[1]Karlsruhe Institute of Technology, [2]George Mason University, [3]Sharif*

	on Thin BOX MOSFET *Hayate Okuhara[1], Kuniaki Kitamor[1], Yu Fujita[1], Kimiyoshi Usami[2], and Hideharu Amano[1]* *[1]Keio University, [2]Shibaura Institute of Technology*	*University of Technology* **10.4.** Power-Efficient Embedded Processing with Resilience and Real-Time Constraints *Liang Wang[1], Augusto Vega[2], Alper Buyuktosunoglu[2], Pradip Bose[2], and Kevin Skadron[1]* *[1]University of Virginia, [2]IBM*
12:15	**ISLPED 2015 Conference Concludes**	

List of Posters

P1. DVAS: Dynamic Voltage Accuracy Scaling for Increased Energy-Efficiency in Approximate Computing
Bert Moons and Marian Verhelst
KU Leuven

P2. Power Management for Mobile Games on Asymmetric Multi-Cores
Anuj Pathania, Santiago Pagani, Muhammad Shafique, and Joerg Henkel
Karlsruhe Institute of Technology (KIT)

P3. An Efficient DVS Scheme for On-Chip Networks Using Reconfigurable Virtual Channel Allocators
Mohammad Sadrosadati[1], Amirhossein Mirhosseini[1], Homa Aghilinasab[1], Hamid Sarbazi-Azad[1, 2]
[1]Sharif University of Technology, [2]Institute for Research in Fundamental Sciences

P4. Having Your Cake and Eating It Too: Energy Savings without Performance Loss through Resource Sharing Driven Power Management
Jae-Yeon Won, Paul Gratz, Srinivas Shakkottai, and Jiang Hu
Texas A&M University

P5. Energy Stealing - An Exploration into Unperceived Activities on Mobile Systems
Chi-Hsuan Lin[1], Yu-Ming Chang[2], Pi-Cheng Hsiu[3], and Yuan-Hao Chang[3]
[1]National Taiwan University, [2]Macronix International Co., Ltd., [3]Academia Sinica

P6. A Win-Win Camera: Quality-Enhanced Power-Saving Images on Mobile OLED Displays
Chih-Kai Kang[1], Chun-Han Lin[2], and Pi-Cheng Hsiu[1]
[1]Academia Sinica, [2]National Taiwan Normal University

P7. Reconfigurable Three Dimensional Photovoltaic Panel Architecture For Solar-Powered Time Extension
Donghwa Shin[1], Naehyuck Chang[2], Yanzhi Wang[3], and Massoud Pedram[3]
[1]Yeungnam University, [2]KAIST, [3]University of Southern California

P8. A micropower energy harvesting circuit with piezoelectric transformer-based ultra-low voltage start-up

Aldo Romani, Antonio Camarda, Alessio Baldazzi, and Marco Tartagni
University of Bologna

P9. Reducing Display Power Consumption for Real-time Video Calls on Mobile Devices
Mengbai Xiao[1], Yao Liu[2], Lei Guo[3], and Songqing Chen[1]
[1]George Mason University, [2]SUNY Binghamton, [3]Ohio State University

P10. A Heuristic Machine Learning-based Algorithm for Power and Thermal Management of Heterogeneous MPSoCs
Arman Iranfar, Soheil Nazar Shahsavani, Mehdi Kamal, and Ali Afzali-Kusha
University of Tehran

P11. ReDEEM: A Heterogeneous Distributed Microarchitecture for Energy-Efficient Reliability
Biruk Mammo, Ritesh Parikh, and Valeria Bertacco
University of Michigan

P12. Post Placement Leakage Reduction with Stress-Enhanced Filler Cells
Jun-Ho Choy[1], Valery Sukharev[1], Armen Kteyan[1], Henrik Hovsepyan[1], Ramnath Venkatraman[2], and Ruggero Castagnetti[2]
[1]Mentor Graphics Corporation, [2]Avago Technologies

P13. Design and Analysis of 6-T 2-MTJ Ternary Content Addressable Memory
Rekha Govindaraj and Swaroop Ghosh
University of South Florida

P14. Modeling and Power Optimization of Cyber-Physical Systems with Energy-Workload Tradeoff
Hoeseok Yang[1] and Soonhoi Ha[2]
[1]Ajou University, [2]Seoul National University

P15. Fixing Sensor-Related Energy Bugs through Automated Sensing Policy Instrumentation
Li Yuanchun, Guo Yao, Kong Junjun, and Chen Xiangqun
Peking University

P16. Analysis and Optimization of CMOS Switched-Capacitor Voltage Converters
Visvesh Sathe[1] and Jae-sun Seo[2]
[1]University of Washington, [2]Arizona State University

P17. The Digital Bidirectional Function as a Hardware Security Primitive:
Teng Xu and Miodrag Potkonjak
University of California, Los Angeles

P18. ThermTap: An Online Power and Thermal Analyzer for Portable Devices
Mohammad Javad Dousti, Majid Ghasemi-Gol, Mahdi Nazmi, and Massoud Pedram
University of Southern California

P19. Lucid Infrared Thermography of Thermally-Constrained Processors
Hussam Amrouch and Joerg Henkel
Karlsruhe Institute of Technology (KIT)

P20. Battery-Aware Energy-Optimal Electric Vehicle Driving Management
Korosh Vatanparvar, Jiang Wan, and Mohammad Al Faruque
University of California, Irvine

P21. Interconnect Synthesis of Heterogeneous Accelerators in Shared Memory
Yu-Ting Chen and Jason Cong
University of California, Los Angeles

P22. Reference-Circuit Analysis for High-Bandwidth Spin Transfer Torque Random Access Memory
Byungkyu Song[1], Taehui Na[1], Seong-Ook Jung[1], Jung Pill Kim[2], Seung H. Kang[2]
[1]Yonsei University, [2]Qualcomm Inc.

ISLPED Gold Sponsors

ISLPED Silver Sponsors

Design Contest Sponsor

Sponsored by:

Technical Support

- from Digital Circuits and Systems Group at Sapienza

- from EvoElectronics