ISLPED 2015 Technical Program

July 22-24, 2015, Rome, Italy

<table>
<tr><th colspan="3">Day 1: Wednesday, July 22, 2015</th></tr>
<tr><td>08:00 – 08:30</td><td colspan="2">Conference Registration</td></tr>
<tr><td>08:30 – 09:00</td><td colspan="2">Welcome by General Co-Chairs and Technical Program Co-Chairs and presentation of the IEEE CASS C.A. Desoer Technical Achievement Award (Room 1)</td></tr>
<tr><td>09:00 – 10:00</td><td colspan="2">Keynote 1: “Let's Get Physical: Adding Physical Dimensions to Cyber Systems,” Alberto Sangiovanni-Vincentelli, University of California, Berkeley (Room 1)
Chair: Luca Benini, ETH Zurich and University of Bologna</td></tr>
<tr><td>10:00 – 10:30</td><td colspan="2">Coffee Break (Cloister)</td></tr>
<tr><td>10:30 – 12:30</td><td>Session 1: Emerging Technologies for Energy Efficiency (Room 1)

1.1. COAST: Correlated Material Assisted STT MRAMs for Optimized Read Operation
Ahmedullah Aziz, Nikhil Shukla, Suman Datta, and Sumeet Gupta
Pennsylvania State University

1.2. A Novel Slope Detection Technique for Robust STTRAM Sensing
Seyedhamidreza Motaman[1], Swaroop Ghosh[1], and Jaydeep Kulkarni[2]
[1]University of South Florida, [2]Intel

1.3. Optimizing Boolean Embedding Matrix for Compressive Sensing in RRAM Crossbar
Yuhao Wang[1], Xin Li[1], Hao Yu[1], Leibin Ni[1], Wei Yang[2], Chuliang Weng[2], and Junfeng Zhao[2]
[1]Nanyang Technological University, [2]Huawei Technologies Co., Ltd

1.4. Fine-Grained Write Scheduling for PCM Performance Improvement under Write Power Budget
Chun-Hao Lai[1], Shun-Chih Yu[1], Chia-Lin Yang[1], and Hsiang-Pang Li[2]
[1]National Taiwan University, [2]MXIC Corp</td><td>Session 2: Thermal Management and Cooling (Cloister Room)

2.1. A Simulation Framework for Rapid Prototyping and Evaluation of Thermal Mitigation Techniques in Many-Core Architectures (Industry Perspectives)
Tanguy Sassolas[1], Chiara Sandionigi[2], Alexandre Guerre[1], Julien Mottin[3], Pascal Vivet[3], Hela Boussetta[4], and Nicolas Peltier[4]
[1]CEA LIST, [2]CEA, [3]CEA LETI, [4]Docea Power

2.2. Making Sense of Thermoelectrics for Processor Thermal Management and Energy Harvesting
Sriram Jayakumar and Sherief Reda
Brown University

2.3. Adaptive Sprinting: How to Get the Most Out of Phase Change Based Passive Cooling
Fulya Kaplan and Ayse Coskun
Boston University

2.4. Experimental Characterization of In-Package Microfluidic Cooling on a System-On-Chip
Wen Yueh, Zhimin Wan, Yogendra Joshi, Saibal Mukhopadhyay
Georgia Institute of Technology</td></tr>
<tr><td>12:30 – 13:30</td><td colspan="2">Lunch (Cloister)</td></tr>
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<table>
<tr><td>13:30 – 15:00</td><td colspan="2"><u>Invited Plenary Talks (Room 1)</u>

I-1. Power Management in the Intel Xeon E5 v3, Bill Bowhill, Intel

I-2. Resonant Clock Designs on the IBM POWER8 and z13 Processors from 2 to 5 GHz, Philip Restle, IBM</td></tr>
<tr><td>15:00 – 16:00</td><td colspan="2">Coffee Break with Posters (Cloister)</td></tr>
<tr><td>16:00 – 18:00</td><td>Session 3: Low Power Memory Organization (Room 1)

3.1. Reducing Dynamic Energy of Set-Associative L1 Instruction Cache by Early Tag Lookup
Wei Zhang, Hang Zhang, and John Lach
University of Virginia

3.2. Bank Stealing For Conflict Mitigation in GPGPU Register File
Naifeng Jing, Shuang Chen, Shunning Jiang, Li Jiang, Chao Li, and Xiaoyao Liang
Shanghai Jiao Tong University

3.3. Leveraging Emerging Nonvolatile Memory in High-Level Synthesis with Loop Transformations
Shuangchen Li[1], Ang Li[2], Yuan Zhe[2], Yongpan Liu[2], Peng Li[3], Guangyu Sun[4], Yu Wang[2], Huazhong Yang[2], and Yuan Xie[1]
[1]University of California, Santa Barbara, [2]Tsinghua University, [3]University of California, Los Angeles, [4]Perking University

3.4. Enabling Energy Efficient Hybrid Memory Cube Systems with Erasure Codes
Shibo Wang, Yanwei Song, Mahdi Bojnordi, and Engin Ipek
University of Rochester</td><td>Session 4: Approximate Computing and Neuromorphic Architectures (Cloister Room)

4.1. Design of Fine-grained Sequential Approximate Circuits using Probability-aware Fault Emulation
David May and Walter Stechele
Technische Universität München

4.2. Hybrid Approximate Multiplier Architectures for Improved Power-Accuracy Trade-offs
Georgios Zervakis, Sotirios Xydis, Kostas Tsoumanis, Dimitrios Soudris, and Kiamal Pekmestzi
National Technical University of Athens (NTUA)

4.3. A Power-Aware Digital Feedforward Neural Network Platform with Backpropagation Driven Approximate Synapses
Jaeha Kung, Duckhwan Kim, and Saibal Mukhopadhyay
Georgia Institute of Technology

4.4. A Neuromorphic Neural Spike Clustering Processor for Deep-Brain Sensing and Stimulation Systems
Beinuo Zhang[1], Zhewei Jiang[1], Qi Wang[1], Jae-sun Seo[2], and Mingoo Seok[1]
[1]Columbia University, [2]Arizona State University</td></tr>
<tr><td>18:30 –</td><td colspan="2">Industry Cocktail Reception, followed by Awards Ceremony (please note that the awards ceremony will start at 7pm), and Industry Reception Dinner (Cloister)</td></tr>
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Day 2: Thursday, July 23, 2015		
08:30 – 09:30	**Keynote 2:** "Opportunities in System Power Management for High Performance Mixed Signal Platforms," Jose Pineda de Gyvez, NXP Semiconductors **(Room 1)** **Chair:** Mauro Olivieri, Sapienza University of Rome	
09:30 – 10:00	**Coffee Break (Cloister)**	
10:00 – 12:00	**Session 5: Energy Efficient On-Chip Communication (Room 1)** **5.1.** High-Efficiency Crossbar Switches using Capacitively Coupled Signaling *Cagla Cakir[1], Ron Ho[2], Jon Lexau[3], and Ken Mai[1]* *[1]Carnegie Mellon University, [2]Altera Corp., [3]Oracle Labs* **5.2.** Tackling Voltage Emergencies in NoC Through Timing Error Resilience *Rajesh JayashankaraShridevi, Dean Michael Ancajas, Koushik Chakraborty, and Sanghamitra Roy* *Utah State University* **5.3.** An Energy Efficient and Low Cross-talk CMOS Sub-THz I/O with Surface-wave Modulator and Interconnect *Yuan Liang[1], Hao Yu[1], Junfeng Zhao[2], Wei Yang[2], and Yuangang Wang[2]* *[1]Nanyang Technological University, [2]Huawei Technologies Co., Ltd.* **5.4.** A Compact Low-Power eDRAM-based NoC Buffer *Cheng Li and Paul Ampadu* *University of Rochester*	**Session 6: Low Power Techniques for Robust and Secure Design; Design Contest Winners (Cloister Room)** **6.1.** Collaborative Gate Implementation Selection and Adaptivity Assignment for Robust Combinational Circuits *Hao He, Jiafan Wang, and Jiang Hu* *Texas A&M University* **6.2.** Analysis of Adaptive Clocking Technique for Resonant Supply Voltage Noise Mitigation *Paul Whatmough[1], Shidhartha Das[2], and David Bull[2]* *[1]Harvard University, [2]ARM Ltd.* **6.3.** Exploring Power Attack Protection of Resource Constrained Encryption Engines using Integrated Low-Drop-Out Regulators *Arvind Singh, Monodeep Kar, Jong Hwan Ko, and Saibal Mukhopadhyay* *Georgia Institute of Technology* **6.4.** (15 min.) *Design Contest Winner:* A 2.89-uW Clockless Fully-Integrated Wireless ECG SoC for Wearable Sensors Xiaoyang Zhang, Zhe Zhang, Yongfu Li, Changrong Liu, Yong Xin Guo and Yong Lian National University of Singapore **6.5.** (15 min.) *Design Contest Winner:* Low Power Detection of Sternocleidomastoid Muscle Contraction for Asthma Assessment and Control *Jun Luan and Pai Chou* *University of California, Irvine*
12:00 – 13:30	**Lunch (Cloister)**	

<table>
<tr><td>13:30 – 15:00</td><td colspan="2"><u>Invited Plenary Talks (Room 1)</u>

I-3. Assessing the Impact of High Power Densities on Aging (title to be confirmed), Joerg Henkel, Karlsruhe Institute of Technology

I-4. Wireless Power Transfer for Implantable Medical Devices, Pedro Irazoqui, Purdue University</td></tr>
<tr><td>15:00 – 15:30</td><td colspan="2">Coffee Break (Cloister)</td></tr>
<tr><td>15:30 – 17:30</td><td>Session 7: Optimizing Power Supply and Delivery (Room 1)

7.1. Fully-Integrated Switched-Capacitor Voltage Regulator with On-Chip Current-Sensing and Workload Optimization in 32nm SOI CMOS
Xiaoyang Mi[1], Debashis Mandal[1], Visvesh Sathe[2], Bertan Bakkaloglu[1], and Jae-sun Seo[1]
[1]Arizona State University, [2]University of Washington

7.2. Modeling and Characterization of the System-Level Power Delivery Network for a Dual-Core ARM Cortex-A57 Cluster in 28nm CMOS (Industry Perspectives)
Shidhartha Das, Paul Whatmough, and David Bull ARM Ltd.

7.3. Transient Voltage Noise in Charge-Recycled Power Delivery Networks for Many-Layer 3D-IC
Runjie Zhang[1], Kaushik Mazumdar[1], Brett Meyer[2], Ke Wang[1], Kevin Skadron[1], and Mircea Stan[1]
[1]University of Virginia, [2]McGill University

7.4. Design and Optimization of a Reconfigurable Power Delivery Network for Large-Area, DVS-Enabled OLED Displays
Woojoo Lee[1], Yanzhi Wang[2], Donghwa Shin[3], Shahin Nazarian[2], and Massoud Pedram[2]
[1]ETRI, [2]University of Southern California, [3]Yeungnam University</td><td>Session 8: Low Power Software and Systems (Cloister Room)

8.1. Hardware-Software Interaction for Run-time Power Optimization: A Case Study of Embedded Linux on Multicore Smartphones (Industry Perspectives)
Anup Das[1], Matthew Walker[1], Andreas Hansson[1,2], Bashir Al-Hashimi[1], and Geoff Merrett[1]
[1]University of Southampton, [2]ARM Ltd.

8.2. CGSharing: Efficient Content Sharing in GPU-Based Cloud Gaming
Xiangyu Wu, Yuanfang Xia, NaifengJing, and Xiaoyao Liang
Shanghai Jiao Tong University

8.3. Energy Efficient Scheduling for Web Search on Heterogeneous MicroServers
Sankalp Jain[1], Harshad Navale[1], Umit Ogras[1], and Siddharth Garg[2]
[1]Arizona State University, [2]New York University

8.4. Low-Power Detection of Sternocleidomastoid Muscle Contraction for Asthma Assessment and Control
Jun Luan, Seungjae Lee, and Pai Chou
University of California, Irvine</td></tr>
<tr><td>17:45 – 19:00</td><td colspan="2">Special Panel for the 20th Anniversary of ISLPED (Room 1)</td></tr>
<tr><td>19:30 -</td><td colspan="2">ISLPED 2015 Banquet and Dinner</td></tr>
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Day 3: Friday, July 24, 2015

08:30 – 09:30	**Keynote 3:** "Statistical Information Processing: Computing For The Nanoscale Era," Naresh Shanbhag, University of Illinois at Urbana Champaign **(Room 1)** **Chair:** Renu Mehra, Synopsys	
09:30 – 10:15	**Coffee Break with Posters (Cloister)**	
10:15 – 12:15	**Session 9: Efficient Power Modeling, Estimation, and Optimization (Room 1)** **9.1.** PowerTrain: A Learning-based Calibration of McPAT Power Models *Wooseok Lee[1], Youngchun Kim[1], Jee Ho Ryoo[1], Dam Sunwoo[2], Andreas Gerstlauer[1], and Lizy K. John[1]* *[1]University of Texas at Austin, [2]ARM R&D* **9.2.** FreqLeak: A frequency step based method for efficient leakage power characterization in a system *Arun Joseph, Anand Haridass, Charles Lefurgy, Sreekanth Pai, Spandana Rachamalla, and Francesco Campisano* *IBM* **9.3.** Power benefit study of monolithic 3D IC at the 7nm technology node *Kyungwook Chang[1], Kartik Acharya[1], Saurabh Sinha[2], Brian Cline[2], Greg Yeric[2], and Sung Kyu Lim[1]* *[1]Georgia Institute of Technology, [2]ARM Inc.* **9.4.** An Optimal Power Supply And Body Bias Voltage for a Ultra Low Power Micro-Controller with Silicon on Thin BOX MOSFET *Hayate Okuhara[1], Kuniaki Kitamor[1], Yu Fujita[1], Kimiyoshi Usami[2], and Hideharu Amano[1]* *[1]Keio University, [2]Shibaura Institute of Technology*	**Session 10: Dynamic Adaptation Techniques for Energy Efficiency (Cloister Room)** **10.1.** Hierarchical Power Budgeting for Dark Silicon Chips *Muhammad Usman Karim Khan, Muhammad Shafique, and Joerg Henkel Karlsruhe Institute of Technology (KIT)* **10.2.** Dynamic Power Management for Many-Core Platforms in the Dark Silicon Era: A Multi-Objective Control Approach *Amir-Mohammad Rahmani[1,2], Mohammad-Hashem Haghbayan[1], Anil Kanduri[1], Awet Yemane Weldezion[2], Pasi Liljeberg[1], Juha Plosila[1], Axel Jantsch[3], and Hannu Tenhunen[1,3]* *[1]University of Turku, [2]KTH Royal Institute of Technology, [3]Vienna University of Technology* **10.3.** DRVS: Power-Efficient Reliability Management through Dynamic Redundancy and Voltage Scaling under Variations *Mohammad Salehi[1], Mohammad Khavari Tavana[2], Semeen Rehman[1], Florian Kriebel[1], Muhammad Shafique[1], Alireza Ejlali[3], and Joerg Henkel[1]* *[1]Karlsruhe Institute of Technology, [2]George Mason University, [3]Sharif University of Technology* **10.4.** Power-Efficient Embedded Processing with Resilience and Real-Time Constraints *Liang Wang[1], Augusto Vega[2], Alper Buyuktosunoglu[2], Pradip Bose[2], and Kevin Skadron[1]* *[1]University of Virginia, [2]IBM*
13:00 - 17:00	**Co-located Workshop:** Nano-Tera Workshop on Ultra-Low Power Environmental monitoring, Security, and Health (ULPESH) Please see http://www.islped.org/2015/workshops.html for details.	

List of Posters (Cloister)

1. DVAS: Dynamic Voltage Accuracy Scaling for Increased Energy-Efficiency in Approximate Computing
Bert Moons and Marian Verhelst
KU Leuven

2. Power Management for Mobile Games on Asymmetric Multi-Cores
Anuj Pathania, Santiago Pagani, Muhammad Shafique, and Joerg Henkel
Karlsruhe Institute of Technology (KIT)

3. An Efficient DVS Scheme for On-Chip Networks Using Reconfigurable Virtual Channel Allocators
Mohammad Sadrosadati[1], Amirhossein Mirhosseini[1], Homa Aghilinasab[1], and Hamid Sarbazi-Azad[1,2]
[1]Sharif University of Technology, [2]Institute for Research in Fundamental Sciences

4. Having Your Cake and Eating It Too: Energy Savings without Performance Loss through Resource Sharing Driven Power Management
Jae-Yeon Won, Paul Gratz, Srinivas Shakkottai, and Jiang Hu
Texas A&M University

5. Energy Stealing - An Exploration into Unperceived Activities on Mobile Systems
Chi-Hsuan Lin[1], Yu-Ming Chang[2], Pi-Cheng Hsiu[3], and Yuan-Hao Chang[3]
[1]National Taiwan University, [2]Macronix International Co., Ltd., [3]Academia Sinica

6. A Win-Win Camera: Quality-Enhanced Power-Saving Images on Mobile OLED Displays
Chih-Kai Kang[1], Chun-Han Lin[2], and Pi-Cheng Hsiu[1]
[1]Academia Sinica, [2]National Taiwan Normal University

7. Reconfigurable Three Dimensional Photovoltaic Panel Architecture For Solar-Powered Time Extension
Donghwa Shin[1], Naehyuck Chang[2], Yanzhi Wang[3], and Massoud Pedram[3]
[1]Yeungnam University, [2]KAIST, [3]University of Southern California

8. A micropower energy harvesting circuit with piezoelectric transformer-based ultra-low voltage start-up
Aldo Romani, Antonio Camarda, Alessio Baldazzi, and Marco Tartagni
University of Bologna

9. Reducing Display Power Consumption for Real-time Video Calls on Mobile Devices
Mengbai Xiao[1], Yao Liu[2], Lei Guo[3], and Songqing Chen[1]
[1]George Mason University, [2]SUNY Binghamton, [3]Ohio State University

10. A Heuristic Machine Learning-based Algorithm for Power and Thermal Management of Heterogeneous MPSoCs
Arman Iranfar, Soheil Nazar Shahsavani, Mehdi Kamal, and Ali Afzali-Kusha
University of Tehran

11. ReDEEM: A Heterogeneous Distributed Microarchitecture for Energy-Efficient Reliability
Biruk Mammo, Ritesh Parikh, and Valeria Bertacco
University of Michigan

12. Post Placement Leakage Reduction with Stress-Enhanced Filler Cells
Jun-Ho Choy[1], Valery Sukharev[1], Armen Kteyan[1], Henrik Hovsepyan[1], Ramnath Venkatraman[2] , and Ruggero Castagnetti[2]
[1]Mentor Graphics Corporation, [2]Avago Technologies

13. Design and Analysis of 6-T 2-MTJ Ternary Content Addressable Memory
Rekha Govindaraj and Swaroop Ghosh
University of South Florida

14. Modeling and Power Optimization of Cyber-Physical Systems with Energy-Workload Tradeoff
Hoeseok Yang[1] and Soonhoi Ha[2]
[1]Ajou University, [2]Seoul National University

15. Fixing Sensor-Related Energy Bugs through Automated Sensing Policy Instrumentation
Li Yuanchun, Guo Yao, Kong Junjun, and Chen Xiangqun
Peking University

16. Analysis and Optimization of CMOS Switched-Capacitor Voltage Converters
Visvesh Sathe[1] and Jae-sun Seo[2]
[1]University of Washington, [2]Arizona State University

17. The Digital Bidirectional Function as a Hardware Security Primitive:
Teng Xu and Miodrag Potkonjak
University of California, Los Angeles

18. ThermTap: An Online Power and Thermal Analyzer for Portable Devices
Mohammad Javad Dousti, Majid Ghasemi-Gol, Mahdi Nazmi, and Massoud Pedram
University of Southern California

19. Lucid Infrared Thermography of Thermally-Constrained Processors
Hussam Amrouch and Joerg Henkel
Karlsruhe Institute of Technology (KIT)

20. Battery-Aware Energy-Optimal Electric Vehicle Driving Management
Korosh Vatanparvar, Jiang Wan, and Mohammad Al Faruque
University of California, Irvine

21. Interconnect Synthesis of Heterogeneous Accelerators in Shared Memory
Yu-Ting Chen and Jason Cong
University of California, Los Angeles

22. Reference-Circuit Analysis for High-Bandwidth Spin Transfer Torque Random Access Memory
Byungkyu Song[1], Taehui Na[1], Seong-Ook Jung[1], Jung Pill Kim[2], Seung H. Kang[2]
[1]Yonsei University, [2]Qualcomm Inc.