Monday, July 24 (Registration hours: 07:45 – 17:20)

<table>
<tr><td>8:00</td><td colspan="2">Breakfast</td></tr>
<tr><td>08:40 – 09:00</td><td colspan="2">Welcome by General and Program Co-Chairs
[Forum Hall]</td></tr>
<tr><td>09:00 – 10:00</td><td colspan="2">Keynote I
A New Silicon Age 4.0: Generating Semiconductor-Intelligence Paradigm with a Virtual Moore's Law Economics and Heterogeneous Technologies
Dr. Nicky Lu
Etron Technology, Inc.

Chair: Chia-Lin Yang (National Taiwan University)
[Forum Hall]</td></tr>
<tr><td>10:00 – 10:30</td><td colspan="2">Coffee Break</td></tr>
<tr><td rowspan="2">10:30 – 11:45</td><td>Session 1A
Memories & their Applications

Session Chair: Sangyoung Park (TU Műnchen)
[Locke Hall]</td><td>Session 1B
Design Implications of Novel Interconnects & Technologies

Session Chair: Alper Buyuktosunoglu (IBM T.J. Watson Research Center)
[Archimedes Hall]</td></tr>
<tr><td>Write-Energy-Saving ReRAM-Based Nonvolatile SRAM with Redundant Bit-Write-Aware Controller for Last-Level Caches
Tsai-Kan Chien[12], Lih-Yih Chiou[1], Yi-Sung Tsou[1], Shyh-Shyuan Sheu[2], Pei-Hua Wang[2], Ming-Jinn Tsai[2] and Chih-I Wu[2]
[1]National Cheng Kung University, [2]Industrial Technology Research Institute

Charge Recycled Low Power SRAM with Integrated Write and Read Assist, for Wearable Electronics, Designed in 7nm FinFET Technology
Vivek Nautiyal, Gaurav Singla,</td><td>A Carbon Nanotube Transistor based RISC-V Processor using Pass Transistor Logic
Best Paper Nominee
Aporva Amarnath, Siying Feng, Subhankar Pal, Tutu Ajayi, Austin Rovinski and Ronald G. Dreslinski
University of Michigan

Architecting Large-Scale SRAM Arrays with Monolithic 3D Integration
Joonho Kong[1], Young-Ho Gong[2] and Sung Woo Chung[2]
[1]Kyungpook National University, [2]Korea University</td></tr>
</table>

	Satinderjit Singh, Fakhruddin ali Bohra, Jitendra Dasani, Lalit Gupta and Sagar Dwivedi *ARM, Ltd.* **Spin-Torque Sensors with Differential Signaling for Fast and Energy Efficient Global Interconnects** *Zubair Azim and Kaushik Roy* *Purdue University*	**Temporal Codes in On-Chip Interconnects** *Michael Mishkin[1], Nam Sung Kim[2] and Mikko Lipasti[1]* *[1]University of Wisconsin-Madison, [2]University of Illinois Urbana-Champaign*
11:45 – 13:15	**Lunch** [Just Italian, 2F, Just Sleep Hotel]	
13:15 – 14:45	**Poster Session** Session Chair: *Thomas Wenisch (University of Michigan)* [Plato Hall]	**Design Contest** Session Chairs: *Saibal Mukhopadhyay (Georgia Tech), Yongpan Liu (Tsinghua University)* [Plato Hall]
	P1. Enabling Efficient Fine-Grained DRAM Activations with Interleaved I/O *Chao Zhang and Xiaochen Guo* *Lehigh University* **P2. Gabor Filter Assisted Energy Efficient Fast Learning Convolutional Neural Networks** *Syed Shakib Sarwar, Priyadarshini Panda and Kaushik Roy* *Purdue University* **P3. Low Design Overhead Timing Error Correction Scheme for Elastic Clock Methodology** *Sungju Ryu, Jongeun Koo and Jae-Joon Kim* *Pohang University of Science and Technology*	**D1. A Low-Power Dual-Core Motion Estimation Chip Design and Implementation for a Wireless Panoramic Endoscopy** *Tsung-Yi Wu and Ching-Hwa Cheng* *Feng Chia University* **D2. An Atomic-Aware Design to Maximize Energy Utilization on NVP-based Self-Powered Sensor Systems** *Chih-Kai Kang[1], Chun-Han Lin[2] and Pi-Cheng Hsiu[1]* *[1]Academia Sinica, [2]National Taiwan Normal University* **D3. High Energy-Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications** *Shouyi Yin, Peng Ouyang, Shibin*

	P4. Efficient Query Processing in Crossbar Memory *Mohsen Imani, Saransh Gupta, Atl Arredondo and Tajana Rosing* *UC San Diego* **P5. A Low Power Duobinary Voltage Mode Transmitter** *Ming-Hung Chien, Yen-Long Lee, Jih-Ren Goh and Soon-Jyh Chang* *National Cheng Kung University* **P6. A Simple Yet Efficient Accuracy Configurable Adder Design** *Wenbin Xu[1], Sachin Sapatnekar[2] and Jiang Hu[1]* *[1]Texas A&M University, [2]University of Minnesota* **P7. E-Spector: Online Energy Inspection for Android Applications** *Chengke Wang, Yao Guo, Peng Shen and Xiangqun Chen* *Peking University* **P8. A Case for Efficient Accelerator Design Space Exploration via Bayesian Optimization** *Brandon Reagen[1], José Miguel Hernanez-Lobato[2], Robert Adolf[1], Michael Gelbart[3], Paul Whatmough[14], Gu-Yeon Wei[1] and David Brooks[1]* *[1]Harvard University, [2]University of Cambridge, [3]University of British Columbia, [4]ARM Research* **P9. SceneMan: Bridging Mobile Apps with System Energy Manager via Scenario Notification** *Li Li[1], Jun Wang[2], Xiaorui Wang[1], Handong Ye[2] and Ziang Hu[2]* *[1]Ohio State University, [2]Huawei Technologies*	*Tang, Fengbin Tu, Xiudong Li, Leibo Liu and Shaojun Wei* *Tsinghua University* **D4. An Ultra-Low Power 169-nA 32.768-kHz Fractional-N PLL** *Chun-Yu Lin, Tun-Ju Wang, Tzu-Hsuan Liu and Tsung-Hsien Lin* *National Taiwan University* **D5. TeleProbe: Zero-Power Contactless Probing for Implantable Medical Devices** *Woo Suk Lee[1], Younghyun Kim[2] and Vijay Raghunathan[3]* *[1]Microsoft, [2]University of Wisconsin-Madison, [3]Purdue University* **D6. Retention State-Aware Energy Management for Efficient Nonvolatile Processors** *Dongqin Zhou[1], Weiwen Chen[1], Xin Shi[2], Mengying Zhao[3] and Keni Qiu[14]* *[1]Capital Normal University, [2]Tsinghua University, [3]Shandong University, [4]Beijing Advanced Innovation Center for Imaging Technology* **D7. 1.4-mW, 56-GHz Arithmetic Logic Unit Based on Superconductor Single-Flux-Quantum Logic Circuit** *Masamitsu Tanaka[1], Ryo Sato[1], Yuki Hatanaka[1], Yuichiro Matsui[1], Hiroyuki Akaike[1], Akira Fujimaki[1], Koki Ishida[2], Takatsugu Ono[2] and Koji Inoue[2]* *[1]Nagoya University, [2]Kyushu University* **D8. A Reconfigurable Building Block for Thermoelectric Generator Energy Harvesting under Spatial**

	P10. Online Tuning of Dynamic Power Management for Efficient Execution of Interactive Workloads *James R. B. Bantock, Vasileios Tenentes, Bashir M. Al-Hashimi and Geoff V. Merrett* *University of Southhampton* **P11. Workload-Driven Frequency-Aware Battery Sizing** *Yukai Chen, Enrico Macii and Massimo Poncino* *Politecnico di Torino* **P12. Exploring Sparsity of Firing Activities and Clock Gating for Energy-Efficient Recurrent Spiking Neural Processors** *Yu Liu, Yingyezhe Jin and Peng Li* *Texas A&M University* **P13. QuARK: Quality-Configurable Approximate STT-MRAM Cache by Fine-Grained Tuning of Reliability-Energy Knobs** *Amir Mahdi Hosseini Monazzah[1], Majid Shoushtari[2], Seyed Ghassem Miremadi[1], Amir M. Rahmani[23] and Nikil Dutt[2]* *[1]Sharif University of Technology, [2]UC Irvine, [3]TU Wien* **P14. Efficient Thermoelectric Cooling for Mobile Devices** *Youngmoon Lee, Eugene Kim and Kang G. Shin* *University of Michigan* **P15. Low Power In-Memory Computing based on Dual-Mode SOT-MRAM** *Farhana Parveen, Shaahin Angizi, Zhezhi He and Deliang Fan* *University of Central Florida*	**Temperature Variations** *Jaemin Kim[1], Naehyuck Chang[2], Donkyu Baek[2], Youngil Kim[2] and Donghwa Shin[3]* *[1]Seoul National University, [2]KAIST, [3]Yeungnam University*

	Session 2A Analog Circuit Design Session Chair: *Shreyas Sen* *(Purdue University)* [Locke Hall]	Session 2B HW Support for CNNs Session Chair: *Ron Dreslinski* *(University of Michigan)* [Archimedes Hall]
14:45 – 16:00	**A 0.13pJ/bit, Referenceless Transceiver with Clock Edge Modulation for a Wired Intra-BAN Communication** *Jihwan Park, Gi-Moon Hong, Mino Kim, Joo-Hyung Chae and Suhwan Kim* *Seoul National University* **A 32nm, 0.65-10GHz, 0.9/0.3 ps/σ TX/RX jitter Single Inductor Digital Fractional-n Clock Generator for Reconfigurable Serial I/O** *William Y. Li, Hyung Seok Kim, Kailash Chandrashekar, Khoa Nguyen, Ashoke Ravi* *Intel Corp.* **A Tunable Ultra Low Power Inductorless Low Noise Amplifier Exploiting Body Biasing of 28 nm FDSOI Technology** *Jennifer Zaini[1], Frédéric Hameau[2], Thierry Taris[1], Dominique Morche[1], Patrick Audebert[1] and Eric Mercier[1]* *[1]CEA Leti, [2]University of Bordeaux*	**CORAL: Coarse-grained Reconfigurable Architecture for Convolutional Neural Networks** *Zhe Yuan, Yongpan Liu, Jinshan Yue, Jinyang Li and Huazhong Yang* *Tsinghua University* **XNOR-POP: A Processing-in-Memory Architecture for Binary Convolutional Neural Networks in Wide-IO2 DRAMs** *Lei Jiang[1], Minje Kim[1], Wujie Wen[2] and Danghui Wang[3]* *[1]Indiana University Bloomington, [2]Florida International University, [3]Northwestern Polytechnical University* **Bit-Width Reduction and Customized Register for Low Cost Convolutional Neural Network Accelerator** *Kyungrak Choi, Woong Choi, Kyungho Shin and Jongsun Park* *Korea University*
16:00 – 16:30	**Coffee Break**	
16:30 – 17:20	**Session 3A** **Energy Storage & Cyber-Physical Systems** Session Chair: *Enrico Macii* *(Politecnico di Torini)* [Locke Hall]	**Session 3B** **Design Methodologies for Machine Learning** Session Chair: *Mikko Lipasti* *(University of Wisconsin-Madison)* [Archimedes Hall]

	Battery Assignment and Scheduling for Drone Delivery Businesses ***Best Paper Nominee*** *Sangyoung Park, Licong Zhang and Samarjit Chakraborty* *TU Műnchen* **Reconfigurable Thermoelectric Generators for Vehicle Radiators Energy Harvesting** *Donkyu Baek[1], Caiwen Ding[2], Sheng Lin[2], Donghwa Shin[3], Jaemin Kim[4], Xue Lin[5], Yanzhi Wang[2] and Naehyuck Chang[1]* *[1]KAIST, [2]Syracuse University, [3]Yeungnam University, [4]Seoul National University, [5]Northeastern University*	**Power Optimizations in MTJ-based Neural Networks through Stochastic Computing** *Ankit Mondal and Ankur Srivastava* *University of Maryland* **A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders** *Subhendu Roy[1], Yuzhe Ma[2], Jin Miao[1] and Bei Yu[2]* *[1]Cadence Design Systems, [2]Chinese University of Hong Kong*
17:30 – 20:00	**Industrial Reception (for all registered attendees)** [Living One, National Taiwan University]	

Tuesday, July 25 (Registration hours: 07:45 – 16:40)

8:00	**Breakfast**	
09:00 – 10:00	**Keynote II** **Peering into the Post Moore's Law World** *Prof. Todd Austin* *University of Michigan* Chair: *Thomas Wenisch (University of Michigan)* [Forum Hall]	
10:00 – 10:30	**Coffee Break**	
10:30 – 11:45	**Session 4A** **Low-Voltage & Energy-Efficient Design**	**Session 4B** **Approximate & Learn!**

	Session Chair: *Naehyuck Chang (KAIST)* [Locke Hall]	Session Chair: *Hsiang-Yun Cheng (Academia Sinica)* [Archimedes Hall]
	Comparative Study and Optimization of Synchronous and Asynchronous Comparators at Near-Threshold Voltages *Sung Justin Kim, Doyun Kim and Mingoo Seok* *Columbia University* **Full Chip Power Benefits with Negative Capacitance FETs** *Sandeep K. Samal[1], Sourabh Khandelwal[2], Asif I. Khan[1], Sayeef Salahuddin[3], Chenming Hu[3] and Sung Kyu Lim[1]* *[1]Georgia Tech, [2]Macquerie University, [3]UC Berkeley* **Design High Bandwidth-Density, Low Latency and Energy Efficient On-Chip Interconnect** *Yong Wang and Hui Wu* *University of Rochester*	**AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing** *Younghyun Kim[1], Setareh Behroozi[1], Vijay Raghunathan[2] and Anand Raghunathan[2]* *[1]University of Wisconsin-Madison, [2]Purdue University* **Approximate Memory Compression for Energy-Efficiency** *Ashish Ranjan, Arnab Raha, Vijay Raghunathan and Anand Raghunathan* *Purdue University* **SENIN: An Energy-Efficient Sparse Neuromorphic System with On-Chip Learning** *Myung-Hoon Choi, Seungkyu Choi, Jaehyeong Sim and Lee-Sup Kim* *KAIST*
11:45 – 13:15	**Lunch** [Just Italian, 2F, Just Sleep Hotel]	
13:15 – 14:30	**Session 5A** **Architecture & Technology Support for Neural Networks** Session Chair: *Tsung-Te Liu (National Taiwan University)* [Locke Hall]	**Session 5B** **Power Delivery** Session Chair: *Pradip Bose (IBM T. J. Watson Research Center)* [Archimedes Hall]
	Monolithic 3D IC Designs for Low-Power Deep Neural Networks Targeting Speech Recognition *Kyungwook Chang[1], Deepak Kadetotad[2], Yu Cao[2], Jae-Sun Seo[2]*	**Placement Mitigation Techniques for Power Grid Electromigration** *Wei Ye[1], Yibo Lin[1], Xiaoqing Xu[1], Wuxi Li[2], Yiwei Fu[2], Yongsheng Sun[2], Canhui Zhan[2] and David Z. Pan[1]*

	and Sung Kyu Lim[1] *[1]Georgia Tech, [2]Arizona State University* **A Programmable Event-Driven Architecture for Evaluating Spiking Neural Networks** *Arnab Roy[1], Swagath Venkataramani[2], Neel Gala[1], Sanchari Sen[2], Kamakoti Veezhinathan[1] and Anand Raghunathan[2]* *[1]IIT Madras, [2]Purdue University* **An Energy-Efficient and High-Throughput Bitwise CNN on Sneak-Path-Free Digital ReRAM Crossbar** *Leibin Ni[1], Zichuan Liu[1], Wenhao Song[2], J. Joshua Yang[2], Hao Yu[1], Kenwen Wang[3] and Yuangang Wang[3]* *[1]Nanyang Technological University, [2]University of Massachusetts Amherst, [3]Huawei Technologies*	*[1]UT Austin, [2]Hisilicon Technologies* **Spatial and Temporal Scheduling of Clock Arrival Times for IR Hot-Spot Mitigation, Reformulation of Peak Current Reduction.** *Bhoopal Gunna, Lakshmi Bhamidipati, Houman Homayoun and Avesta Sasan* *George Mason University* **Frequency and Time Domain Analysis of Power Delivery Network for Monolithic 3D ICs** *Kyungwook Chang[1], Shidhartha Das[2], Saurabh Sinha[2], Brian Cline[2], Greg Yeric[2] and Sung Kyu Lim[1]* *[1]Georgia Tech, [2]ARM*
14:30 – 15:00	**Coffee Break**	
15:00 – 16:40	**Session 6A** **Multi-Scale Energy-Efficient Designs** Session Chair: *Yiran Chen (Duke University)* [Locke Hall]	**Session 6B (Special Session)** **Interaction of Power Management & Security** Session Chair: *Hsien-Hsin Sean Lee (TSMC)* [Archimedes Hall]
	ShiftMask: Dynamic OLED Power Shifting Based on Visual Acuity for Interactive Mobile Applications *Han-Yi Lin[1], Pi-Cheng Hsiu[2] and Tei-Wei Kuo[1 2]* *[1]National Taiwan University, [2]Academia Sinica*	**(Invited) Ultra-low Energy Security Circuit Primitives for IoT Platforms** *Sanu Mathew, Sudhir Satpathy, Vikram Suresh and Ram Krishnamurthy* *Intel Labs*

	Signal Strength-Aware Adaptive Offloading for Energy Efficient Mobile Devices *Young Geun Kim and Sung Woo Chung* *Korea University* **Frequency Governors for Cloud Database OLTP Workloads** *Rathijit Sen and Alan Halverson* *Microsoft* **Tiguan: Energy-Aware Collision-Free Control for Large-Scale Connected Vehicles** *Minghua Shen and Guojie Luo* *Peking University*	**(Invited) Low Power Requirements and Side-Channel Protection of Encryption Engines: Challenges and Opportunities** *Monodeep Kar[1], Arvind Singh[1], Sanu Mathew[2], Anand Rajan[2], Vivek De[2] and Saibal Mukhopadhyay[1]* *[1]Georgia Tech, [2]Intel Labs* **(Invited) Resilient and Energy-Secure Power Management** *Pradip Bose and Alper Buyuktosunoglu* *IBM T. J. Watson Research Center* **(Invited) Secure Swarm Intelligence: A New Approach to Many-Core Power Management** *Augusto Vega, Alper Buyuktosunoglu and Pradip Bose* *IBM T. J. Watson Research Center*
17:30 – 21:00	**Banquet** [Kunlun Hall, 12F, The Grand Hotel] * Buses bound for the banquet venue will depart from the main gate of NTU at 17:00.	

Wednesday, July 26 (Registration hours: 07:45 – 12:00)

8:00	**Breakfast**
09:00 – 10:00	**Keynote III** **Architecture and Software for Emerging Low-Power Systems** *Prof. Wen-Mei W. Hwu* *University of Illinois Urbana-Champaign* Chair: *David Garrett (Broadcom)* [Forum Hall]
10:00 – 10:30	**Coffee Break**

	Session 7A **Emerging Technologies** Session Chair: *David Brooks* *(Harvard University)* [Locke Hall]	Session 7B **Low-Power HW Security** Session Chair: *Sanu Mathew* *(Intel Labs)* [Archimedes Hall]
10:30 – 11:45	**Transistor-Level Monolithic 3D Standard Cell Layout Optimization for Full-Chip Static Power Integrity** *Bon Woong Ku[1], Taigon Song[2], Arthur Nieuwoudt[2] and Sung Kyu Lim[1]* *[1]Georgia Tech, [2]Synopsys* **Secure Human-Internet Using Dynamic Human Body Communication** *Shovan Maity, Debayan Das, Xinyi Jiang and Shreyas Sen* *Purdue University* **Hotspot Monitoring and Temperature Estimation with Miniature On-Chip Temperature Sensors** *Pavan Kumar Chundi, Yini Zhou, Martha Kim, Eren Kursun and Mingoo Seok* *Columbia University*	**A Data Remanence based Approach to Generate 100% Stable Keys from an SRAM Physical Unclonable Function** ***Best Paper Nominee*** *Muqing Liu, Chen Zhou, Qianying Tang, Keshab K. Parhi and Chris H. Kim* *University of Minnesota* **An Improved Clocking Methodology for Energy Efficient Low Area AES Architectures using Register Renaming** *Siva Nishok Dhanuskodi and Daniel Holcomb* *University of Massachusetts Amherst* **A Low-Power APUF-based Environmental Abnormality Detection Framework** *Hongxiang Gu, Teng Xu and Miodrag Potkonjak* *UC Los Angeles*
11:45 – 12:00	**Closing Remarks** [Forum Hall]	
12:00 – 12:30	**Sack Lunch**	
12:30	**Embedded Tutorial** **Tiny Light-Harvesting Photovoltaic Charger-Supplies** *Gabriel A. Rincón-Mora* *Georgia Tech* 12:30 – 15:30 [Locke Hall]	**Excursions** **(Optional, tickets can be purchased at the online registration system)** Excursion A - Yilan (12:30 – 21:30) Excursion B - Hsinchu (12:30 – 19:30) * Buses bound for Yilan and Hsinchu will depart from the main gate of NTU at 12:30.