



Updated on August 4

ISLPED 2023

**INTERNATIONAL
SYMPOSIUM ON
LOW POWER
ELECTRONICS AND
DESIGN**

AUGUST 7–8, 2023, TU WIEN, VIENNA, AUSTRIA



LOGISTICS

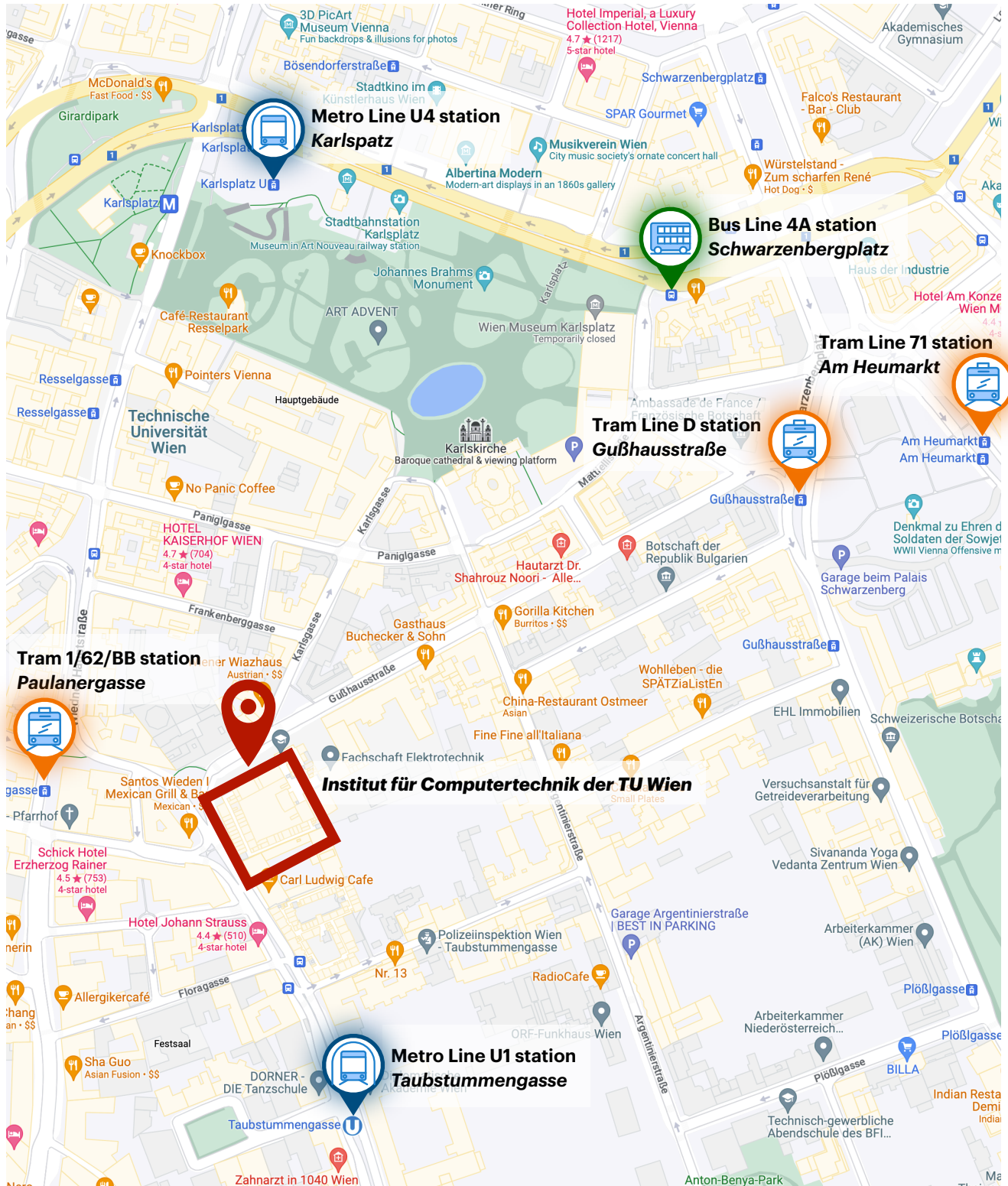
Welcome Reception and Conference (Sunday to Tuesday)

Institut für Computertechnik der TU Wien

Address: Gußhausstr. 27-29, 1040 Vienna

Welcome Reception (Sun) @ Rooftop (6th floor)

Conference (Mon/Tue) @ Ground floor

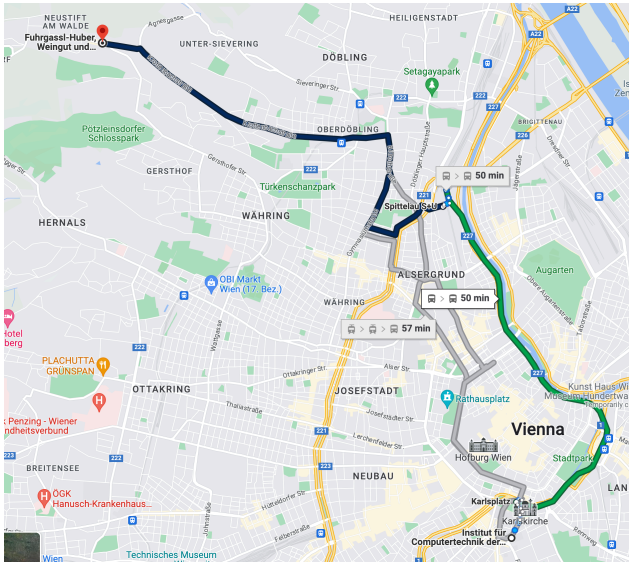


Banquet Dinner (Monday)
Fuhrgassl-Huber, Weingut und Buschenschank
 Address: Neustift am Walde 68, 1190 Vienna

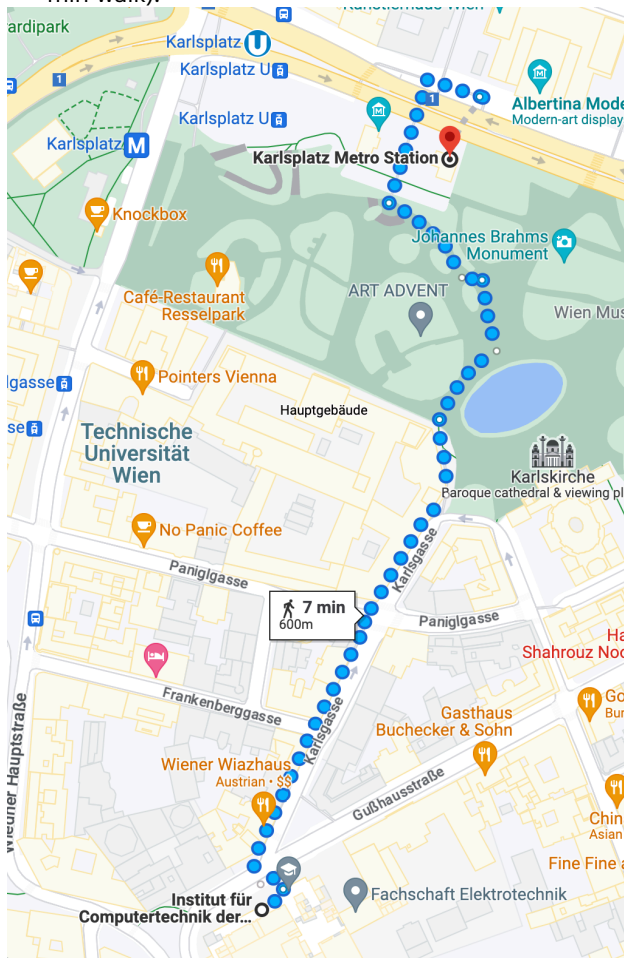


Public Transportation Guide

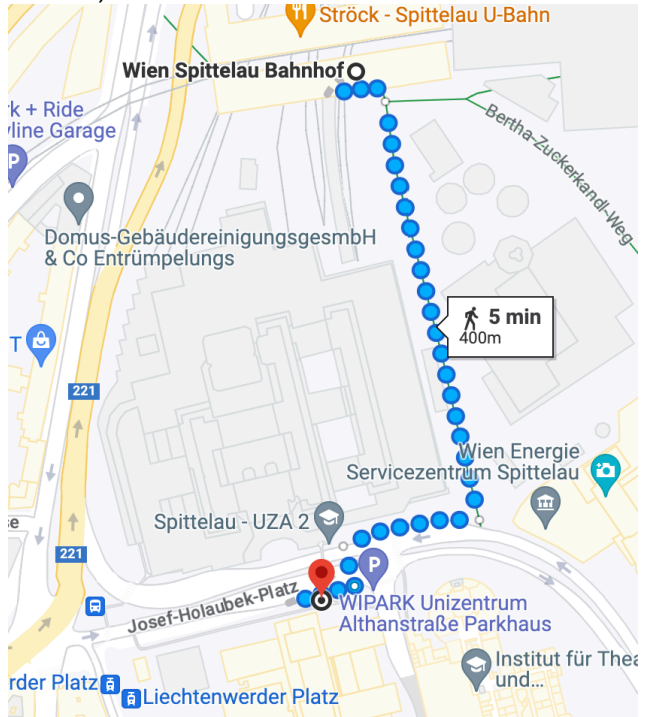
Overall route from the conference site to the restaurant.



1. Take Metro Line **U4** at **Karlsplatz** station (600 m, 7 min walk).



2. Get off at **Spittelau** station (10 min, 7 stops). Take Bus Line **35A** at **Spittelau S+U** station (400 m, 5 min walk).



3. Get off at **Neustift am Walde** station (21 min, 16 stops). The restaurant is 1 min walk ahead.



PROGRAM OVERVIEW

E18 E18 Pötzl E19 E19 Hlawka

Sunday, August 6		
18:00–22:00	Welcome Reception (6th floor rooftop)	
Monday, August 7		
7:30–8:00	Registration	
8:00–8:30	Welcome E18	
8:30–9:30	Keynote 1 E18 Radu Marculescu <i>"Thirty Years of Low-Power Design: From Watts to Wisdom"</i>	
9:30–9:45	Coffee Break	
9:45–10:45	Special Session E18 Aida Todri-Sanial, Sudeep Pasricha, and Partha Pande (Organizer) <i>"Energy-Efficient ML Acceleration: From Technologies to Circuits and Systems"</i>	
10:45–11:00	Coffee Break	
11:00–12:20	Session 1A E18 <i>"Energy-Efficient Memory and Processing"</i>	Session 1B E19 <i>"Performance- and Energy-Aware Acceleration and Tensor Processing"</i>
12:20–14:00	Lunch (Main Hall) & Poster Session (Side Hall)	
14:00–15:00	Design Contest E18	
15:00–15:10	Coffee Break	
15:10–16:30	Session 2A E18 <i>"Energy-Efficient Sensors, Processors, and Middleware"</i>	Session 2B E19 <i>"Energy-Efficient Hardware Acceleration of GNN and Transformers"</i>
16:30–19:30	Break	
19:30–	Banquet Dinner Buschenschank Fuhrgassl-Huber	
Tuesday, August 8		
7:30–8:00	Registration	
8:00–9:00	Keynote 2 E18 Jan Rabaey <i>"Lessons from the Brain"</i>	
9:00–9:10	Coffee Break	
9:10–10:40	Panel Discussion E18 Massoud Pedram (Organizer), Ajay Joshi (Moderator), Ahmed Hemani, Axel Jantsch, Diana Marculescu, Radu Marculescu, and Aida Todri-Sanial <i>"Artificial General Intelligence: A Technological Marvel or an Existential Question"</i>	
10:40–10:50	Coffee Break	
10:50–12:10	Session 3A E18 <i>"ML-Driven Automation and Multi-Objective Optimization for Low-Power Design"</i>	Session 3B E19 <i>"Novel Processing-in-Memory Techniques for Low Power"</i>
12:10–13:50	Lunch (Main Hall) & Poster Session (Side Hall)	
13:50–15:10	Session 4A E18 <i>"When Low Power Design Meets Hardware Security"</i>	Session 4B E19 <i>"Low Power AI Accelerators and AI for Low Power Design"</i>
15:10–15:20	Coffee Break	
15:20–16:20	Session 5A E18 <i>"Novel Parallel Architectures for Deep Learning"</i>	
16:20–16:30	Closing Remarks and Awards E18	

MONDAY PROGRAM

8:30–9:30 E18 Pötzl	Keynote 1 Chair: Umit Ogras, University of Wisconsin–Madison
	<i>Thirty Years of Low-Power Design: From Watts to Wisdom</i> Radu Marculescu, University of Texas at Austin
9:45–10:45	Special Session Organizer: Partha Pande, Washington State University
	<i>Energy-Efficient ML Acceleration: From Technologies to Circuits and Systems</i> Aida Todri-Sanial, Eindhoven University of Technology Sudeep Pasricha, Colorado State University Partha Pande (Organizer), Washington State University
11:00–12:20 E18 Pötzl	Session 1A: “Energy-Efficient Memory and Processing” Chair: Alexander Fish, Bar-Ilan University
11:00–11:20	<i>A Comparative Study on Front-Side, Buried and Back-Side Power Rail topologies in 3nm technology node</i> Sandra Shaji, Lingjun Zhu, Junsik Yoon and Sung Kyu Lim
11:20–11:40	<i>CoolDRAM: An Energy-Efficient and Robust DRAM (Best Paper Candidate)</i> Nezam Rohbani, Mohammad Arman Soleimani and Hamid Sarbazi-Azad
11:40–12:00	<i>Development of Tropical Algebraic Accelerator with Energy Efficient Time-Domain Computing for Combinatorial Optimization and Machine Learning</i> Qiankai Cao, Xi Chen and Jie Gu
12:00–12:20	<i>IMBUE: In-Memory Boolean-to-Current Inference Architecture for Tsetlin Machines</i> Omar Ghazal, Simranjeet Singh, Tousif Rahman, Shengqi Yu, Yujin Zheng, Domenico Balsamo, Sachin Patkar, Farhad Merchant, Fei Xia, Alex Yakovlev and Rishad Shafiq
11:00–12:20 E19 Hlawka	Session 1B: “Performance- and Energy-Aware Acceleration and Tensor Processing” Chair: Ganapati Bhat, Washington State University
11:00–11:20	<i>iMAT: Energy-Efficient In-Memory Acceleration of Ternary Neural Networks With Sparse Dot Product (Best Paper Candidate)</i> Shien Zhu, Shuo Huai, Guochu Xiong and Weichen Liu
11:20–11:40	<i>Accelerating ML-adjacent Computation Using Tensor Processors</i> Dongho Ha, Won Woo Ro and Hung-Wei Tseng
11:40–12:00	<i>Energy-Harvesting-Aware Adaptive Inference of Deep Neural Networks in Embedded Systems</i> Gwanjong Park, Osama Khan and Euseong Seo
12:00–12:20	<i>Precision-aware Latency and Energy Balancing on Multi-Accelerator Platforms for DNN Inference</i> Matteo Riso, Alessio Burrello, Giuseppe Maria Sarda, Luca Benini, Enrico Macii, Massimo Poncino, Marian Verhelst and Daniele Jahier Pagliari
12:20–14:00	Lunch & Poster Session
Main Hall (Lunch) Side Hall (Posters)	List of posters on p. 9
14:00–15:00 E18 Pötzl	Design Contest Co-Chairs: Rajesh Kedia, IIT Hyderabad; Florian Huemer, TU Wien
14:00–14:03	<i>Energy Aware Time Series Classification for Low-Power Microcontrollers</i> Matthias Bittner, Dominik Dallinger, Matthias Wess, Daniel Schnoell, and Axel Jantsch

14:03–14:06	A Low-Power RISC-V Multicore Processor with a Shared Lightweight FPU Jina Park, Eunjin Choi, Woojoo Lee, Sukho Lee, Jae-Jin Lee, and Massoud Pedram
14:06–14:09	SmartHeaP - A High-level Programmable, Low Power, and Mixed-Signal Hearing Aid SoC in 22nm FD-SOI Jens Karrenbauer, Simon Klein, Sven Schönewald, Lukas Gerlach, Meinolf Blawat, Jens Benndorf and Holger Blume
14:09–14:12	Object Detection on a Nano-Drone Using a RISC-V Multi-Core MCU Accelerator Luca Bompani, Lorenzo Lamberti, Victor Javier Kartsch, Manuele Rusci, Daniele Palossi and Luca Benini
14:12–14:15	PLP-DVS: Adaptive Energy Scaling of Capacitor-Based Power Loss Protection in SSDs Jaehyuck Cho, Jeongmin Jeongmin Choi, Sunghyun Park, Jiyong Kim, Sungjun Yun, Kyungmin Lim, Jaehyun Park, Sungyong Ahn, and Donghwa Shin
14:15–14:18	A Passive Bidirectional BLE Tag Demonstrating Battery-Free Communication in Tablet/ Smartphone-to-Tag, Tag-to-Tablet/Smartphone, and Tag-to-Tag Modes Ziyi Chang, Qijing Xiao, Cheng Chen, Yuxuan Luo, and Bo Zhao
14:18–14:21	TunnelTx: Demonstrating Low-Power Wireless Transmissions using Tunnel Diode based Wireless Transmitters Wenqing Yan, Manoj Gulati, Prabal Dutta, and Ambuj Varshney
14:21–15:00	Live demo and poster presentation
15:10–16:30 E18 Pötzl	Session 2A: “Energy-Efficient Sensors, Processors, and Middleware” Chair: Jaehyun Park, University of Ulsan
15:10–15:30	Florian: Developing a Low-power RISC-V Multicore Processor with a Shared Lightweight FPU Jina Park, Kyuseung Han, Eunjin Choi, Sukho Lee, Jae-Jin Lee, Woojoo Lee and Massoud Pedram
15:30–15:50	Energy Efficient Real-Time Scheduling on Heterogeneous Architectures with Self-Suspension Model Wenwen Xu, Zheyu Zhang, Yuankai Xu, Jing Li, Yehan Ma, Yier Jin, Chris Gill, Xuan Zhang and An Zou
15:50–16:10	CARMA: Context-Aware Runtime Reconfiguration for Energy-Efficient Sensor Fusion Yifan Zhang, Arnav Malawade, Xiaofang Zhang, Yuhui Li, DongHwan Seong, Mohammad Al Faruque and Sitao Huang
16:10–16:30	Uncertainty-aware Online Learning for Dynamic Power Management in Large Manycore systems (Best Paper Candidate) Gaurav Narang, Raid Ayoub, Michael Kishinevsky, Jana Doppa and Partha Pratim Pande
15:10–16:30 E19 Hlawka	Session 2B: “Energy-Efficient Hardware Acceleration of GNN and Transformers” Chair: Nee Arman Roohi, University of Nebraska
15:10–15:30	A Multicore GNN Training Accelerator Sudipta Mondal, Ramprasath S, Ziqing Zeng, Kishor Kunal and Sachin S. Sapatnekar
15:30–15:50	Joint Optimization of Cache Management and Graph Reordering for GCN Acceleration Kyeong-Jun Lee, ByungJun Kim, Han-Gyeol Mun, Seunghyun Moon and Jae-Yoon Sim
15:50–16:10	ITA: An Energy-Efficient Attention and Softmax Accelerator for Quantized Transformers Gamze Islamoglu, Moritz Scherer, Gianna Paulin, Tim Fischer, Victor Jung, Angelo Garofalo and Luca Benini
16:10–16:30	Energy-Efficient RISC-V-Based Vector Processor for Cache-Aware Structurally-Pruned Transformers Jung Gyu Min, Dongyun Kam, Younghoon Byun, Gunho Park and Youngjoo Lee

TUESDAY PROGRAM

8:00–9:00	Keynote 2
E18 Pötzl	Chair: Pascal Meinerzhagen, Intel Corporation
	Lessons from the Brain Jan M. Rabaey, University of California, Berkeley
9:10–10:40	Panel Discussion
E18 Pötzl	Organizer: Massoud Pedram, University of Southern California; Moderator: Ajay Joshi, Boston University and Lightmatter
	Artificial General Intelligence: A Technological Marvel or an Existential Question Massoud Pedram (Organizer), University of Southern California Ajay Joshi (Moderator), Boston University and Lightmatter Ahmed Hemani, KTH Royal Institute of Technology Axel Jantsch, Technische Universität Wien Diana Marculescu, University of Texas at Austin Radu Marculescu, University of Texas at Austin Aida Todri-Sanial, Technische Universiteit Eindhoven
10:50–12:10	Session 3A: “ML-Driven Automation and Multi-Objective Optimization for Low-Power Design”
E18 Pötzl	Chair: Massimo Poncino, Politecnico di Torino
10:50–11:10	Machine Learning Driven Synthesis of Clock Gating Doyeon Won, Soomin Kim and Taewhan Kim
11:10–11:30	Automatic Generation of Cell Based Structured CIM Macros Christian Lanius, Jie Lou, Johnson Loh and Tobias Gemmeke
11:30–11:50	Multi-objective optimization for Floating Point Mix-Precision Tuning (Best Paper Candidate) Zeqing Li and Youhui Zhang
11:50–12:10	REFROM: Responsive, Energy-efficient Frame Rendering for Mobile Devices (Best Paper Candidate) Tsong-Yen Hsu, Yi-Shen Chen, Yun-Chih Chen, Yuan-Hao Chang and Tei-Wei Kuo
10:50–12:10	Session 3B: “Novel Processing-in-Memory Techniques for Low Power”
E19 Hlawka	Chair: Yoav Weizman, Bar-Ilan University
10:50–11:10	CIM-3DRec: A 3D Reconstruction Accelerator with Digital Computing-in-Memory and Octree-Based Scheduler Yiqi Jing, Yiyang Sun, Xiao Wang, Wentao Zhao, Meng Wu, Fengyun Yan, Yufei Ma, Le Ye and Tianyu Jia
11:10–11:30	Processing-in-Memory using Optically-Addressed Phase Change Memory Guowei Yang, Cansu Demirkiran, Zeynep Ece Kizilates, Carlos A. Rios Ocampo, Ayse Coskun and Ajay Joshi
11:30–11:50	LAXOR: A Bit-Accurate BNN Accelerator with Latch-XOR Logic for Local Computing (Best Paper Candidate) Dongrui Li, Tomomasa Yamasaki, Niangjun Chen, Mani Aarthy, Anh Tuan Do and Bo Wang
11:50–12:10	AR-PIM: An Adaptive-Range Processing-in-Memory Architecture Teyuh Chou, Fernando Garcia-Redondo, Paul Whatmough and Zhengya Zhang
12:10–13:50	Lunch & Poster Session
Main Hall (Lunch) Side Hall (Posters)	List of posters on p. 9
13:50–15:10	Session 4A: “When Low Power Design Meets Hardware Security”
E18 Pötzl	Chairs: Ajay Joshi, Boston University

- 13:50–14:10 **Low Power Logic Obfuscation Through System Level Clock Gating**
Daniel Xing, Yuntao Liu and Ankur Srivastava
- 14:10–14:30 **FPGA-Patch: Mitigating Side Channel Attacks on Multi-Tenant FPGAs using Dynamic Patch Generation (Best Paper Candidate)**
Mahya Morid Ahmadi, Lilas Alrahis, Ozgur Sinanoglu and Muhammad Shafique
- 14:30–14:50 **Enabling DVFS Side-Channel Attacks for Neural Network Fingerprinting in Edge Inference Services**
Erich Malan, Valentino Peluso, Andrea Calimera and Enrico Macii
- 14:50–15:10 **Hardware Trojans in fdSOI**
Christian Lanius, Florian Freye, Shutao Zhang and Tobias Gemmeke
- 13:50–15:10 Session 4B: “Low Power AI Accelerators and AI for Low Power Design”**
EI9 Hlawka Chair: Younghyun Kim, University of Wisconsin–Madison
- 13:50–14:10 **Bridging the Gap between Spiking Neural Networks & LSTMs for Latency & Energy Efficiency**
Gourav Datta, Haoqin Deng, Robert Aviles, Zeyu Liu and Peter Beerel
- 14:10–14:30 **Partial-sum Quantization for near ADC-Less Compute-In-Memory Accelerators**
Utkarsh Saxena and Kaushik Roy
- 14:30–14:50 **Efficient Multi-Objective Optimization for PVT Variation-Aware Circuit Sizing using Surrogate Models and Smart Corner Sampling**
Octavian Pascu, Catalin Visan, Georgian Nicolae, Mihai Boldeanu, Horia Cucu, Cristian V. Diaconu, Andi Buzo and Georg Pelz
- 14:50–15:10 **Model-Driven Dataset Generation for Data-Driven Battery SOH Models**
Khaled Sidahmed Sidahmed Alamin, Francesco Daghero, Giovanni Pollo, Daniele Jahier Pagliari, Yukai Chen, Enrico Macii, Massimo Poncino and Sara Vinco
- 15:20–16:20 Session 5A: “Novel Parallel Architectures for Deep Learning”**
EI8 Pötzl Chair: Jiang Hu, Texas A&M University
- 15:20–15:40 **Ocellus: Highly Parallel Convolution-in-Pixel Scheme Realizing Power-Delay-Efficient Edge Intelligence (Best Paper Candidate)**
Sepehr Tabrizchi, Shaahin Angizi and Arman Roohi
- 15:40–16:00 **Sky-NN: Enabling Efficient Neural Network Data Processing with Skyrmion Racetrack Memory**
Yong-Cheng Liao, Shuo-Han Chen, Yuan-Hao Chang and Yu-Pei Liang
- 16:00–16:20 **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit**
Hyun Woo Oh, Seongmo An, Won Sik Jeong and Seung Eun Lee

POSTERS

Monday 12:20–14:00 & Tuesday 12:10–13:50

- 1 **Scaled Population Division for Approximate Computing**
Kunal Bharathi, Sunil Khatri and Jiang Hu
- 2 **Cryogenic CMOS as an Enabler for Low Power Dynamic Logic**
Rakshith Saligram, Suman Datta and Arijit Raychowdhury
- 3 **Quantifying the Overheads of Modular Multiplication**
Deepraj Soni, Mohammed Nabeel Thari Moopan, Negar Neda, Ramesh Karri, Michail Maniatakos and Brandon Reagen
- 4 **Multi-Source Transfer Learning for Design Technology Co-Optimization**
Jakang Lee, Jaeseung Lee, Seonghyeon Park and Seokhyeong Kang
- 5 **Enabling Highly-Efficient DNA Sequence Mapping via ReRAM-based TCAM**
Yu-Shao Lai, Shuo-Han Chen and Yuan-Hao Chang
- 6 **A Self-powered Predictive Maintenance System Based on Piezoelectric Energy Harvesting and TinyML**
Zijie Chen, Yiming Gao and Junrui Liang
- 7 **Temperature-Aware Memory Mapping and Active Cooling of Neural Processing Units**
Vahidreza Moghaddas, Hammam Kattan, Tim Buecher, Mikail Yayla, Jian-Jia Chen and Hussam Amrouc
- 8 **WeNet: Configurable Neural Network with Dynamic Weight-Enabling for Efficient Inference**
Jingxiao Ma and Sherief Reda
- 9 **Energy-Efficient Missing Data Recovery in Wearable Devices: A Novel Search-based Approach**
Dina Hussein, Taha Belkhouja, Ganapati Bhat and Jana Doppa
- 10 **RecPIM: A PIM-Enabled DRAM-RRAM Hybrid Memory System For Recommendation Models**
Heewoo Kim, Haojie Ye, Trevor Mudge, Ronald Dreslinski and Nishil Talati
- 11 **Weight-Aware Activation Mapping for Energy-Efficient Convolution on PIM Arrays**
Kang Eun Jeon, Johnny Rhe, Hyeonsu Bang and Jong Hwan Ko
- 12 **Teleport: A High-Performance ShiftNet Hardware Accelerator with Fused Layer Computation**
Hyunmin Kim and Sungju Ryu
- 13 **Energy-Efficient ReRAM-based ML Training via Mixed Pruning and Reconfigurable ADC**
Chukwufumnanya Ogbogu, Biresh Kumar Joardar, Soumen Mohapatra, Jana Doppa, Deukhyoun Heo, Krishnendu Chakrabarty and Partha Pratim Pande
- 14 **Digital Implementation of On-Chip Hebbian Learning for Oscillatory Neural Networks**
Edgar Leonard Marvin Luhulima, Madeleine Abernot, Federico Corradi and Aida Todri-Sanial
- 15 **PAIRS: Pruning-Aided Row-Skipping for SDK-Based Convolutional Weight Mapping in Processing-In-Memory Architectures**
Johnny Rhe, Kang Eun Jeon and Jong Hwan Ko
- 16 **A Fully-Integrated Energy-Scalable Transformer Accelerator Supporting Adaptive Model Configuration and Word Elimination for Language Understanding on Edge Devices**
Zexi Ji, Hanrui Wang, Miaorong Wang, Win-San Khwa, Meng-Fan Chang, Song Han and Anantha P. Chandrakasan
- 17 **Learning from Output Transitions: A Chosen Challenge Strategy for ML Attacks on PUFs**
Chia-Chih Lin and Ming-Syan Chen
- 18 **Efficient Machine Learning on Encrypted Data using Hyperdimensional Computing**
Yujin Nam, Minxuan Zhou, Saransh Gupta, Gabrielle De Micheli, Rosario Cammarota, Chris Wilkerson, Daniele Micciancio and Tajana Rosing

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TECHNICAL PROGRAM COMMITTEE

Track 1. Technology, Circuits, and Architecture

1.1–1.2. Technologies and Circuits

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Rahul Rao (Track Co-Chair), IBM
Deliang Fan, Arizona State University
Fady Abouzeid, ST Microelectronics
Frank Gurkaynak, ETH Zurich
Sudhanshu Khanna, Texas Instruments
Vishal Khatri, Kandou
Amit Agarwal, Intel
Alexandre Levisse, EPFL
Farshad Moradi, Aarhus University
Joycee Mekie, IIT Gandhinagar
Inhee Lee, University of Pittsburgh

1.3. Logic and Architecture

Antonia Zhai (Track Co-Chair), University of Minnesota
John (Jack) Sampson (Track Co-Chair), Pennsylvania State University
Adam Teman, Bar-Ilan University
Daniel Wong, UC Riverside
Marisa Lopez-Vallejo, Universidad Politécnica de Madrid
Matthias Korb, ETH Zurich
Theocharis Theocharides, University of Cyprus
M. Hassan Najafi, University of Louisiana
Kshitij Bhardwaj, LLNL

Track 2. CAD, Systems, and Software

2.1. CAD Tools and Methodologies

Enrico Macii (Track Co-Chair), Politecnico di Torino
Azadeh Davoodi (Track Co-Chair), University of Wisconsin-Madison
Alberto Macii, Politecnico di Torino
Pascal Vivet, CEA-Leti
Matthew Ziegler, IBM
Alessio Burrello, University of Bologna
Francesco Regazzoni, USI
Donkyu Baek, Chungbuk National University
Nadine Azemard-Crestani, LIRMM
Sanghamitra Roy, Utah State University

2.2. Systems and Platforms

Marina Zapater (Track Co-Chair), University of Applied Sciences Western Switzerland
Hun Seok Kim (Track Co-Chair), University of Michigan
Donghwa Shin, Soongsil University
Massimo Poncino, Politecnico di Torino
Pai Chou, National Cheng Kung University, Taiwan
Jaehyun Park, University of Ulsan
Mohammad Al Faruque, UC Irvine
Masanori Hashimoto, Osaka University
Hussam Amrouch, University of Stuttgart
Taeyoung Kim, Intel
Jason Xue, City University of Hong Kong
William Fornaciari, Politecnico di Melano
Ganapati Bhat, Washington State University

2.3. Software and Applications

Yuan-Hao Chang (Track Co-Chair), Academia Sinca
Xue Lin (Track Co-Chair), North Eastern University
Ittetsu Taniguchi, Osaka University
Wanli Chang, University of York
Daniele Jahier Pagliari, Politecnico di Torino
Young Geun Kim, Korea University
Aporva Amarnath, IBM
Jalil Boukhobza, ENSTA-Bretagne

Track 3. AI/ML Hardware and System Security

3.1. AI/ML Hardware

Aida Todri-Sanial (Track Co-Chair), CNRS-LIRMM/University of Montpellier
Priyadarshini Panda (Track Co-Chair), Yale
Jan Moritz Joseph, RWTH
Amit Trivedi, University of Illinois
Georgios Karakonstantis, Queen's University Belfast
Arman Roohi, University of Nebraska
Kanad Basu, University of Texas Dallas
Gokul Krishnan, Arizona State University
Prabal Basu, Cadence
Abhronil Sengupta, Pennsylvania State University
Shaahin Angizi, New Jersey Institute of Technology
Youngjoo Lee, POSTECH
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Nikita Mirchandani, On Semi
Jae-sun Seo, Arizona State University
Greg Chen, Intel
Phil Knag, Intel
Cedric Lichtenau, IBM
Sumit Mandal, Indian Institute of Science
Jae-Yoon Sim, POSTECH

3.2. Hardware and System Security

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Kaveh Shamsi, University of Texas Dallas
Wei Jiang, UESTC
Asmit De, SiFive
Sara Tehranipoor, West Virginia University
Debjyoti Bhattacharjee, IMEC
Debayan Das, Intel
Shivam Bhasin, Nanyang Technological University
Sohrab Aftabjahani, Intel
Jeyavijayan Rajendran, Texas A&M University