

CALL FOR PAPERS ISLPED 2024

INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

<http://www.islped.org>



Hyatt Regency Newport Beach, California, USA

August 5–7, 2024



Organizing Committee and Symposium Officers:

General Chair

Pascal Meinerzhagen, *Intel*
pascal.a.meinerzhagen@intel.com

Program Co-Chairs

Kapil Dev, *Nvidia*
kdev@nvidia.com
Jerald Yoo, *Seoul National University*
[jyoo@ieee.org](mailto: jyoo@ieee.org)

Local Arrangements Chair

Mehdi Kamal, *USC*
mehdi.kamal@usc.edu

Treasurer

Mehdi Kamal, *USC*
mehdi.kamal@usc.edu

Publications Chair

Younghyun Kim, *Univ. Wisconsin*
younghyun.kim@wisc.edu

Web/Registration Co-Chairs

Meron Demissi, *UMich*
mdemissi@umich.edu
Ganapati Bhat, *WSU*
ganapati.bhat@wsu.edu

Publicity Co-Chairs

Semeen Rehman, *TU Wien*
semeen.rehman@tuwien.ac.at
Jaeha Kung, *Korea Univ.*
jhkung@korea.ac.kr
Linghao Song, *UCLA*
linghaosong@cs.ucla.edu

Design Contest Co-Chairs

Rajesh Kedia, *IITH*
rkedia@cse.iith.ac.in
Payam Heydari, *UCI*
payam.heydari@uci.edu

Industry Liaison Co-Chairs

Adam Teman, *BIU*
adam.teman@biu.ac.il
Amlan Ganguly, *RIT*
axgeec@rit.edu

Sponsored by the **ACM Special Interest Group on Design Automation (SIGDA)**, the **IEEE Circuits and Systems Society (CASS)**, the **IEEE Solid-State Circuits Society (SSCS)** and the **IEEE Council on Electronic Design Automation (CEDA)**.

The International Symposium on Low Power Electronics and Design (ISLPED) is the premier forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, AI/ML-enhanced EDA/CAD, system-level design, and optimization, to system software and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

1. Technology, Circuits, and Architecture	2. EDA, Systems, and Software
1.1. Technologies Low-power technologies for device, interconnect, logic, memory, 2.5/3D, cooling, harvesting, sensors, optical, printable, biomedical, battery, and alternative energy storage devices and technology enablers for non-Boolean and quantum/quantum-inspired compute models.	2.1. CAD Tools and Methodologies CAD tools, methodologies, and AI/ML-based approaches for low-power and thermal-aware design (analog/digital). AI/ML for acceleration of circuit simulation and IP block design convergence. Power estimation, optimization, reliability, and variation impact on power optimization at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.
1.2. Circuits Low-power circuits for logic, memory, reliability, yield, clocking, resiliency; low-power analog/mixed-signal circuits for wireless, RF, MEMS, ADC/DAC, I/O, PLLs/DLLs, DC-DC converters; energy-efficient circuits for emerging applications (e.g., neuromorphic, biomedical, in-vitro sensing, autonomous); circuits using emerging technologies; cryogenic circuits. DTCO for low power; combinatorial optimizers (Ising machine).	2.2. Systems and Platforms Low-power, power-aware, and thermal-aware system design including data centers, SoCs, embedded systems, Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability. Applications of AI/ML-based solutions and brain-inspired computing to power-aware system and platform design.
1.3. Logic and Architecture Low-power logic and microarchitecture for SoC designs, processor cores (compute, graphics, and other special purpose cores), cache, memory, arithmetic/signal processing, cryptography, variability, asynchronous design, and non-conventional computing. System technology co-optimization (STCO) for low power.	2.3. Software and Applications Energy-efficient, energy/thermal-aware software and application design, including scheduling and management, power optimization through HW/SW co-design, and emerging low-power AI/ML applications.
3. Crosscutting Topics	
3.1. AI/ML Hardware, Compute-in-Memory (CIM) and Next-Generation Computing Low-power AI/ML HW techniques including approximations, application driven optimizations, in-memory/near-memory/energy-efficient accelerations, and neuromorphic computing; energy-efficient HW and systems for generative AI applications (LLMs, diffusion models); energy-efficient AI/ML HW using emerging technologies (including quantum computing); analog/mixed-signal computing.	
3.2. Hardware and System Security Low-power hardware security primitives (PUF, TRNG, cryptographic/post-quantum cryptographic accelerators), nano-electronics security, supply chain security, IoT security and AI/ML security; confidential computing; energy-efficient approaches to system security.	
4. Industrial Design Track This track solicits papers to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs.	

Technical Paper Submission Deadlines: [Abstract registration by March 4, 2024](#) [March 11, 2024, at 11:59pm PST](#)
[Full paper due by March 11, 2024](#) [March 18, 2024 at 11:59pm PST](#)

Invited Talk, Panel, and Embedded Tutorial Proposals Deadline: [April 8, 2024](#)

Notification of Paper Acceptance: [May 20, 2024](#)

Submission of Camera-Ready Papers: [June 17, 2024](#)

Submission site: <https://softconf.com/n/islped2024/>

Submissions (not published/accepted/under review by another journal, conference, symposium, or workshop) should be full-length papers of **up to 6 pages** (PDF format, double-column, US letter size, using the ACM proceedings "sigconf" template), available at (<https://www.acm.org/publications/proceedings-template>) including all illustrations, tables, references, and an abstract of no more than 250 words. **Submissions must be anonymous.** Submissions failing above requirements will be automatically rejected. Accepted papers will be submitted to the IEEE Xplore Digital Library and the ACM Digital Library. ISLPED'24 will present three Best Paper Awards based on the ratings of reviewers and a panel of judges.

ISLPED also features a Low Power Design Contest with live demonstrations and awards. Submissions are due on May 13, 2024. More details will soon be available on the conference web page.

There will be several invited talks by industry and academic thought leaders on key issues in low power electronics and design. The Symposium may also include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions in low power electronics and design. Proposals for invited talks, embedded tutorials, and panels should be sent by email to the ISLPED'24 Technical Program Co-Chairs, Kapil Dev (kdev@nvidia.com) and Jerald Yoo (jyoo@nus.edu.sg) by the deadline listed above.

Participants interested in exhibiting at the Symposium should contact the General Chair by April 29, 2024.

Additional notes to authors:

1. "By submitting your article to an ACM Publication, you are hereby acknowledging that you and your co-authors are subject to all ACM Publications Policies, including ACM's new Publications Policy on Research Involving Human Participants and Subjects. Alleged violations of this policy or any ACM Publications Policy will be investigated by ACM and may result in a full retraction of your paper, in addition to other potential penalties, as per ACM Publications Policy."
2. "Please ensure that you and your co-authors obtain an ORCID ID, so you can complete the publishing process for your accepted paper. ACM has been involved in ORCID from the start and we have recently made a commitment to collect ORCID IDs from all of our published authors. The collection process has started and will roll out as a requirement throughout 2022. We are committed to improve author discoverability, ensure proper attribution and contribute to ongoing community efforts around name normalization; your ORCID ID will help in these efforts."
3. Authors may use generative AI software tools to prepare the paper. However, you must disclose their use in either the acknowledgements section of the work or elsewhere in the work prominently. Please refer to the following FAQ webpage for more information about the ACM publication policies: <https://www.acm.org/publications/policies/frequently-asked-questions>