



ISLPED 2025

International Symposium on Low Power Electronics and Design

www.islped.org
University of Iceland, Reykjavik, Iceland
August 6-8, 2025

Organizing Committee

General Chairs

Kapil Dev, Nvidia
kdev@nvidia.com
Jerald Yoo, Seoul National Univ.
jerald@snu.ac.kr

Program Co-Chairs

Younghyun Kim, Purdue Univ.
younghyun@purdue.edu
Srividhya Venkataraman, AMD
srividhya.venkataraman@amd.com

Treasurer

Mehdi Kamal, USC
mehdi.kamal@usc.edu

Publications Chair

Xue Lin, Northwestern Univ.
xue.lin@northeastern.edu

Web/Registration Co-Chairs

Ganapati Bhat, WSU
ganapati.bhat@wsu.edu
Meron Demissie, Univ. of Michigan
mdemissi@umich.edu

Publicity Co-Chairs

Kshitij Bhardwaj, LLNL
bhardwaj2@llnl.gov
Alessio Burrello
alessio.burrello@polito.it
Jinho Lee, Seoul National Univ.
leejinho@snu.ac.kr

Design Contest Co-Chairs

Rajesh Kedia, IIT Hyderabad
rkedia@cse.iith.ac.in
Arnab Raha, Intel
arnab.raha@intel.com

Industry Liaison Co-Chairs

Amlan Ganguly, RIT
axgeec@rit.edu
Renu Mehra, Synopsys
renu.mehra@synopsys.com
Adam Teman, Bar-Ilan Univ.
adam.teman@biu.ac.il

Women in Technology Co-Chairs

Priya Panda, Yale Univ.
priya.panda@yale.edu
Kathy Hoover, AMD
kathy.hoover@amd.com

Important Dates

Technical Papers (11:59 PST)

Abstract registration: March 3 10, 2025

Full paper: March 17, 2025

Invited Talk, Embedded Tutorial, and Panel Proposals
April 7, 2025

Design Contest Applications

May 12, 2025

Notification of Acceptance

May 19, 2025

Camera-ready Submission

June 16, 2025

Submission Site

<https://softconf.com/p/islped2025>

The **International Symposium on Low Power Electronics and Design (ISLPED)** is the premier forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, AI/ML-enhanced EDA/CAD, system-level design, and optimization, to system software and applications. Specific topics include, but are not limited to, the following three main tracks and sub-areas:

Track 1. Technology, Circuits, and Architecture

1.1. Technologies and Circuits

Low-power technologies for device, interconnect, logic, memory, 2.5/3D, cooling, harvesting, sensors, optical, printable, biomedical, battery, and alternative energy storage devices and technology enablers for non-Boolean and quantum/quantum-inspired compute models. Low-power circuits for logic, memory, reliability, yield, clocking, resiliency; low-power analog/mixed-signal circuits for wireless, RF, MEMS, ADC/DAC, I/O, PLLs/DLLs, DC-DC converters; energy-efficient circuits for emerging applications (e.g., neuromorphic, biomedical, in-vitro sensing, autonomous); circuits using emerging technologies; cryogenic circuits. DTCO for low power; combinatorial optimizers (Ising machine). AI/ML-based circuit optimization; circuit architecture for power-efficient AI applications.

1.2. Logic and Architecture

Low-power logic and microarchitecture for SoC designs, processor cores (compute, graphics, and other special purpose cores), cache, memory, arithmetic/signal processing, cryptography, variability, asynchronous design, and non-conventional computing. System technology co-optimization (STCO) for low power. AI/ML-assisted logic optimization and architecture exploration. Power efficient architecture for AI.

Track 2. EDA, Systems, and Software

2.1. CAD Tools and Methodologies

CAD tools, methodologies, and AI/ML-based approaches for low power and thermal-aware design (analog/digital). AI/ML for acceleration of IP block design convergence. Power estimation, optimization, reliability, and variation impact on power optimization at all levels of design abstraction: physical, circuit, gate, register transfer, behavior, and algorithm.

2.2. Systems and Platforms

Low-power, power-aware, and thermal-aware system design including data centers, SoCs, embedded systems, Internet-of-Things (IoT), wearable computing, body-area networks, wireless sensor networks, and system-level power implications due to reliability and variability. Applications of AI/ML-based solutions and brain-inspired computing to power-aware system and platform design.

2.3. Software and Applications

Energy-efficient, energy/thermal-aware software and application design, including scheduling and management, power optimization through HW/SW co-design, and emerging low-power AI/ML applications.

Track 3. Crosscutting Topics

3.1. AI/ML Hardware and Systems

Low-power AI/ML HW techniques including approximations, application-driven optimizations, energy-efficient accelerations, and neuromorphic computing; energy-efficient HW and systems for generative AI applications (LLMs, diffusion models)

3.2. Emerging and Next-Generation Computing

Energy-efficient in-memory/near-memory/in-storage computing; quantum computing; analog/mixed-signal computing; optical computing; bio-inspired computing

3.3. Hardware and System Security

Low-power hardware security primitives (PUF, TRNG, cryptographic/post-quantum cryptographic accelerators), nano-electronics security, supply chain security, IoT security and AI/ML security; confidential computing; energy-efficient approaches to system security.

Track 4. Industrial Design Track

This track solicits papers to reinforce interaction between the academic research community and industry. Industrial Design track papers have the same submission deadline as regular papers and should focus on similar topics but are expected to provide a complementary perspective to academic research by focusing on challenges, solutions, and lessons learnt while implementing industrial-scale designs.

Submissions (not published/accepted/under review by another journal, conference, symposium, or workshop) should be full-length papers of **up to 6 pages** (PDF format, double-column, US letter size, using the IEEE Conference format available at <https://www.ieee.org/conferences/publishing/templates.html>) including all illustrations, tables, and an abstract of no more than 250 words, plus **an additional 1 page for references only**.

Accepted papers will be submitted to the IEEE Xplore Digital Library and the ACM Digital Library. ISLPED'25 will present three Best Paper Awards based on the ratings of reviewers and a panel of judges. Select papers will be invited to submit an extended version for publication in the **IEEE Transactions on Very Large Scale Integration**.

There will be several invited talks by industry and academic thought leaders on key issues in low power electronics and design. The Symposium may also include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions in low power electronics and design. Proposals for invited talks, embedded tutorials, and panels should be sent by email to the ISLPED'25 Technical Program Co-Chairs by the deadline listed on the left. Participants interested in exhibiting at the Symposium should contact the General Chairs by April 30, 2025.

Additional Notes to Authors

- **Author Responsibility:** Submitters must obtain consent from all co-authors for the submission of the manuscript and ensure that their correct author information is provided by the abstract registration deadline.
- **Changes to Author List:** After abstract registration, changes to the author list—including additions, removals, or reordering of authors—are not permitted. However, the corresponding author may be changed up until the camera-ready submission deadline.
- **Anonymity Requirements:** Submissions must be anonymous. Authors' names or affiliations must not appear in the manuscript or the registered abstract. References to the authors' prior work must be cited in the third person, and phrases such as "omitted for blind review" are not allowed in the reference section. PDF metadata must not include any author information. Submissions that fail to meet these blind-review requirements will be automatically rejected without review.
- **Formatting Guidelines:** The manuscript must not exceed 6 pages (excluding references) and must follow the IEEE style template without significant modification. This includes maintaining the specified margins, line spacing, and using a double-column format in 9- or 10-point font. Submissions must be in PDF format, readable, and adhere to the template requirements.
- **Additional Reference Page:** References may be included within the 6-page limit or on one additional page. Inclusion of any non-reference content on the reference page will result in desk rejection. The manuscript and reference page must be combined into a single PDF file.
- **Submission Consistency:** The content and length of the submitted manuscript must not be significantly different to those of the camera-ready version, if accepted.
- **Use of Generative AI Software:** According to the IEEE Publication Services and Products Board Operations Manual, the use of content generated by AI (including but not limited to text, figures, images, and code) shall be disclosed in the acknowledgments section. The AI system used shall be identified, and specific sections of the article that use AI-generated content shall be identified and accompanied by a brief explanation regarding the level at which the AI system was used to generate the content. The use of AI systems for editing and grammar enhancement is common practice and, as such, is generally outside the intent of this policy. In this case, disclosure as noted above is recommended.