ISLPED 06 Proposal for half-day Tutorial

Leakage Currents in Nanometer CMOS

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Abstract: In only 5 years, leakage developed from an academic corner phenomenon to a central problem of embedded system design. In sub *90nm* designs the leakage power will be larger than the dynamic power. The intention of this tutorial is to present the state-of-the-art in leakage modelling, estimation and reduction methodologies.

Schedule

Leakage physics (40 min): From a transistor view, the known sources of leakage are reviewed and their dependencies on physical parameters as temperature, voltage-levels at the terminals, length width and thickness of the structures, doping level, etc. The introduction to the basics of leakage currents enables deeper understanding of the later parts dealing with estimation and optimization of the leakage currents.

- **Subthreshold current** including drain induced barrier lowering (**DIBL**) and other short channel effects (**SCE**'s). Especially thermal threshold voltage, body voltage and source voltage dependence is discussed.
- **Gate leakage** presenting an easy quantum-mechanical introduction to the tunnel-effect and discussing different oxide tunnelling mechanisms. Especially influence of gate-voltage, temperature and oxide thickness needs further attention.
- **PN-junction leakage** carried by 3 mechanisms: drift, electron-hole generation and band to band tunnelling (**BTBT**) with a focus on gate induced drain leakage (**GIDL**) which will make PN-junction leakage becoming the second largest part in the total leakage budget within the next years.
- **Hot carrier injection (HCI)** and **Punchthrough**, both having minor impact will be briefly reviewed for the sake of completeness.

Leakage estimation state-of-the-art (30 min): Existing estimation approaches from device- to system-level are presented. Their strengths and limitations are discussed. Especially:

- The device-level **BSIM** model, which can be included to Berkeley SPICE. BSIM simulations have highest available estimation accuracy, but they need to employ Monte-Carlo simulation to support variation of the process-parameters. As even a single computation of a circuit, apart from trivial cases, can last unacceptably long, Monte Carlo simulations are prohibitive for component-sized or larger circuits.

- Gate level estimation approaches are presented trying to speed up simulation time, abstracting from the explicit CMOS structure but lacking statistical properties.
- On RTL and higher levels, use-case estimators are presented, also offering statistical estimation, but lacking of accuracy and support of optimization techniques.

[Break (30min)**]**

A high-level leakage estimation flow (20 min): As leakage estimation on all levels of abstraction has major limitations, we present the modelling flow developed by the consortium: Starting with a gate-level model considering influence and variation of all important parameters – and the application of different low-leakage and leakage-management techniques, we present how the models can be abstracted to RT-components and even entire IP-blocks with low accuracy degradation and without loosing the awareness of parameters, variations and optimizations.

Design for low leakage (50 min): Here we present several design techniques reducing leakage in active mode – i.e. while the component is working.

- On **physical level** the component structure or the doping profiles can be modified to improve leakage behaviour without diminishing performance.
- On **transistor level**, the 2 most promising leakage management techniques are: Adaptive body biasing (**ABB**) and power gating (**DTCMOS**) which can be implemented in several ways (P-gating, N-gating, ZCMOS, SCCMOS).
- The optimization approaches on **high level** optimize the selection of supply- and body-voltage, try to minimize the peak temperature or to reduce the number of components.

[Discussion (10 min)]