



CALL FOR PAPERS
ISLPED 2009 (<http://www.islped.org>)



INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN
San Francisco, California, August 19 - 21, 2009

Sponsored by **ACM SIGDA** and **IEEE Circuits and Systems Society** with technical support from the **IEEE Solid-State Circuits Society** and the **IEEE Electron Devices Society**. The International Symposium on Low Power Electronics and Design (ISLPED) is the premier forum for presentation of recent advances in all aspects of low power design and technologies, ranging from process and circuit technologies, simulation and synthesis tools, to system level design and optimization. Specific topics include, but are not limited to, the following two main areas, each with **three sub-areas**:

Executive Committee and Symposium Officers

General Co-Chairs:
 Jörg Henkel
 University of Karlsruhe
henkel@informatik.uni-karlsruhe.de

Ali Keshavarzi
 TSMC
alikh@tsmc.com

Program Co-Chairs:
 Naehyuck Chang
 Seoul National University
naehyuck@snu.ac.kr

Tahir Ghani
 Intel
tahir.ghani@intel.com

Local Arrangement Co-chairs:
 Subramani Kengeri
 TSMC
skengeri@tsmc.com

Hamid Mahmoodi
 SFSU
mahmoodi@sfsu.edu

Panel Chair:
 Suman Datta
 Penn State University
sdatta@engr.psu.edu

Special Session Chair:
 Partha Ranganathan
 HP
Partha.Ranganathan@hp.com

Treasurer:
 Yuan Xie
 Penn State University
yuanxie@cse.psu.edu

Publicity Co-Chairs:
 Farzan Fallah
 Envis Corporation
farzan@envis.com

Vijay Raghunathan
 Purdue University
vr@ecn.purdue.edu

Design Contest Chairs:
 Kevin (Yu) Cao
 Arizona State University
Yu.Cao@asu.edu

Chris Kim
 University of Minnesota
chriskim@umn.edu

Exhibits Co-Chairs:
 Vasantha Erraguntla
 Intel
vasantha.erraguntla@intel.com

Qing Wu
 SUNY University, Binghamton
qw@binghamton.edu

Web Chair:
 Yung-Hsiang Lu
 Purdue University
yunglu@purdue.edu

1. Architecture, Circuits, and Technology	2. Design Tools, System and Software Design
1.1. Technologies and Digital Circuits Emerging logic/memory technologies and applications; Low power device and interconnect design; Low power low leakage circuits; Memory circuits; Noise reduction; 3-D technologies; Cooling technologies; Battery technologies; Variation-tolerant design; Temperature-aware and reliable design	2.1. Design Tools Energy simulation and estimation tools that operate at the circuit/gate level, RT level, behavioral level, and algorithmic level; Variation-aware design; Physical design and interconnects
1.2. Logic and Microarchitecture Design Processor core design; Cache and register file design; Logic and RTL design; Arithmetic and signal processing circuits; Encryption technologies; Asynchronous design	2.2. System Design and Methodologies Microprocessor, DSP and embedded systems design; FPGA and ASIC designs; System-level power- and thermal-aware design; System-level reliability- and variability-aware design
1.3. Analog, MEMS, Mixed Signal and Imaging Electronics RF circuits; Wireless; MEMS circuits; AD/DA Converters; I/O circuits; Mixed signal circuits; Imaging circuits; Analog noise; Circuits to support emerging technologies; DC-DC converters	2.3. Software Design and Optimization Power- and thermal-aware software design, scheduling, and management; Application-level optimizations; Wireless and sensor networks; Emerging applications

Submissions on new topics: emerging technologies, architectures/platforms, and applications are particularly encouraged.

TECHNICAL PAPER SUBMISSIONS:

Submissions should be full-length papers of up to 6 pages (double-column format, font size 9pt to 10pt), including all illustrations, tables, references and an abstract of no more than 100 words. Papers exceeding the six-page limit and/or identifying the authors will be automatically rejected. Electronic submission in **PDF format** only via the web is required. More information on electronic submission to ISLPED'09 can be found at <http://www.islped.org>.

Submitted papers must describe original work that will not be announced or published prior to the Symposium and that is not being considered or under review by another conference at the same time. Accepted papers will be presented in one of two parallel tracks: one focusing on architectures, circuits and technologies, the other on design tools and systems and software design for low power. Accepted papers will be published in the Symposium Proceedings and included in the ACM Digital Library. Authors of a few selected papers from the Symposium will also be given an opportunity to submit enhanced versions of their papers for publication in a special issue of a reputed journal. ISLPED'09 will present two Best Paper Awards based on the ratings of reviewers and an invited panel of judges.

IMPORTANT DATES:

- ✓ Technical paper submission deadline: March 20, 2009
- ✓ Invited talks, panels and tutorial proposals deadline: April 13, 2009
- ✓ Notification of paper acceptance: May 11, 2009
- ✓ **Camera-ready version due: June 9, 2009**
- ✓ Exhibition proposal deadline: May 29, 2009
- ✓ Low-power design contest submission deadline: June 5, 2009

INVITED TALKS, PANELS, AND TUTORIAL PROPOSALS:

There will be several invited talks by industry and academic leaders on key issues in low power electronics and design. All invited talks will be in plenary sessions. The Symposium also may include embedded tutorials to provide attendees with the necessary background to follow recent research results, as well as panel discussions on future directions and design/technology alternatives in low power electronics and design. Proposals for invited talks, embedded tutorials, and the panel should be sent to Technical Program Co-Chairs: Naehyuck Chang, Seoul National University, naehyuck@snu.ac.kr and Tahir Ghani, Intel, tahir.ghani@intel.com.

LOW-POWER DESIGN CONTEST:

Low Power Design Contest to provide a forum for universities and research organizations to showcase original **power-aware** designs and to highlight the innovations and design choices targeted at low power. The goal is to encourage and highlight design-oriented approaches to power reduction. Entries identifying the authors will be automatically rejected. Entries should be submitted electronically in **PDF format** only to the Design Contest Chairs: Kevin (Yu) Cao, Arizona State University, Yu.Cao@asu.edu and Chris Kim, University of Minnesota, chriskim@umn.edu.

EXHIBITION APPLICATIONS:

Companies interested in exhibiting at the Symposium should contact the Exhibits Co-Chairs: Vasantha Erraguntla, Intel, vasantha.erraguntla@intel.com and Qing Wu, SUNY University, Binghamton qw@binghamton.edu.

Other Members of the EC:

- B. Barton, Texas Instruments
- D. Blaauw, Univ. of Michigan
- R. Brodersen, UC Berkeley
- A. Chandrakasan, MIT

- K. Choi, Seoul National Univ.
- J. Cong, UCLA
- V. De, Intel Corporation
- G. DeMicheli, EPFL
- C. Enz, CSEM
- M. J. Irwin, Penn State Univ.

- R. Joshi, IBM
- E. Macii, Poli di Torino
- R. Marculescu, CMU
- F. Najm, University of Toronto
- V. Narayanan Penn State U.
- W. Nebel, Oldenberg U.

- M. Pedram, USC
- C. Piguet, CSEM
- J. Rabaey, UC Berkeley
- A. Raghunathan, NEC
- K. Roy, Purdue University
- T. Sakurai, Univ. of Tokyo

- M. Stan, U. of Virginia
- C. Svensson, Linkoping Univ.
- V. Tiwari, Intel Corp.
- I. Verbauwhede, K.U.Leuven