ISLPED 2009

THEME: GREEN DATA CENTERS AND COMPUTING

OVERVIEW AND HIGHLIGHT

ISLPED 2009 Contacts:

General Conference Chairs: Ali Keshavarzi, TSMC and Jörg Henkel, University of Karlsruhe in Germany
Technical Program Committee Chairs: Tahir Ghani, Intel Corporation and Naehyuck Chang, Seoul National University of Korea

Conference Overview:

The technical papers and invited talks at this year's International Symposium on Low Power Electronics and Design (ISLPED 2009) & (www.islped.org) in the San Francisco Bay Area that is scheduled for August 19 through August 21 form a very exciting program for this year's low power symposium (ISLPED). The theme of this year's conference revolves around green electronics covering specifically **green data centers and green computing** in specially designed sessions with distinguished guests from the industry and academic researchers. The conference organizing committee has arranged for a set of complementary embedded (free of charge to conference participants) tutorials that accompanies these special session topics allowing for the symposium participants to probe more into the fundamentals and learn by interacting more on these hot topics. Students and interested professionals are welcomed to take part in the tutorial sessions.

This year's ISLPED conference has a set of 4 industrial **keynote** and **plenary** talks covering a range of topics. Dr. Percy Gilbert (VP of Technology Development at **IBM**) will discuss his views on power performance SoC design and their requirements for advanced process technologies and the necessary design ecosystem that makes their strategy successful.

Dr. Kevin Zhang (Fellow and Director of Advanced Circuit Design at **Intel** Corporation) covers the opportunities and challenges of circuit design in nano CMOS era with Intel's state-of-the-art 32nm HKMG process technology and beyond.

Newly formed **GLOBALFOUNDRIES** executive, Dr. Moji Chian (Senior VP of Design) will outline the opportunities in future low power design enablement and the challenges they will confront.

The well-known fables IP provider **VirageLogic** executive, Dr. Yankin Tanurhan (VP of Engineering and Design) speaks about means to deal with disaggregation in ever-changing world of semiconductors.

These are an array of exciting keynote speeches that once added to the details of the arranged special sessions and the competitively selected technical papers adds value to the experience of the symposium participants.

The special session on **green data centers** has 4 invited talks:
1. Cullen Bash of **HP** expands on sustainable data centers and IT ecosystem.
2. John carter discusses **IBM**'s green data center research activities.
3. Prof. Massoud Pedram of **USC** talks about minimizing data center cooling and server power costs.
4. Prof. Tom Wenisch of University of **Michigan** focuses on system level power management.

The topics at **green computing** special session start with a very special guest from Japan. Dr. Itoh-san of **Hitachi** discusses leakage and variability conscious circuit design for very aggressively scaled power supply voltage of around 0.5V. Al Fazio, a Fellow at **Intel**, follows Dr. Itoh's talk by explaining how Non-Volatile Memories (NVM) can be used for overall system power scaling. Finally Prof. Suman Datta of **Penn State** University discusses very energy efficient logic applications using novel tunneling-based devices.

An industry-oriented **panel** discussion covers low power and power analysis/trade-offs along the traditional focus of the conference with participants from **Cadence, Mentor Graphics, NXP, Broadcom and IDT**.

Selected Technical Paper Overviews:

Some of highlighted technical papers at ISLPED 2009 are listed below:

Paper by Intel - (2.2.1 session)
Title: Dynamic Thermal Management using Thin-Film Thermoelectric Cooling Technology (TEC)
This paper uses forward looking cooling strategies to help with design power envelop that allows for continuous performance scaling.

Paper by National Taiwan University and IBM – (2.2.1 session)
Title: PPT: Joint Performance/Power/Thermal Management of DRAM Memory for Multi-Core Systems
Power in the required high speed and high capacity memory in multi-core architecture systems is critical. This paper focuses on a power-aware memory subsystem design for these architectures by orchestrating task execution and paging allocations while adapting to system loading.

Paper by University of Michigan and IBM – (1.1.2 session)
Title: Low Power Circuit Design based on Heterojunction Tunneling Transistors (HETTs).

This paper targets ultra low power design applications by using a steep subthreshold swing tunneling SiGe heterojunction transistor that improves transistor turn-off properties to achieve very low power.

Paper by University of California at San Diego – (2.3.1 session)
Title: vGreen: A System for Energy Efficient Computing in Virtualized Environments
vGreen works based on a multi-tiered software system for energy efficient computing that boosts the system performance by 20% while saving system energy by 15% for physical or virtualized server machines.

Paper by HP Labs – (2.3.1 session)
Title: Tracking the Power in an Enterprise Decision Support System
Power cost of required IT in enterprise decision support systems motives this paper to suggest optimizing energy use without sacrificing performance by database software based on the workloads. This paper shows holistic measurements of an audit-class system running the TPC-H decision support benchmark at 300GB scale.

Paper by University of Connecticut – (1.2.1 session)
Title: Way-Tagged Cache: An Energy-Efficient L2 Cache Architecture under Write-Through Policy
This paper proposes a cache architecture for high performance microprocessors that lowers the energy consumption of the soft error required write-through policy deployed caches.

Paper from Georgia Tech and ARM – (1.2.1 session)
Title: Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches.
This paper discusses a technique for cache power reduction.

Technical paper highlight and most significant results:

- Continuous performance scaling by dynamic thermal management using emerging thin-film thermoelectric cooling technology (TEC)
- vGreen describes a multi-tiered software system for energy efficient computing that boosts the system performance by 20% while saving system energy by 15% for physical or virtualized server machines
- Ultra low power design is probed by using a steep subthreshold swing tunneling SiGe heterojunction transistor that improves transistor turn-off properties to achieve very low power
- Power in the required high speed and high capacity memory in multi-core architecture systems is critical. A power-aware memory subsystem design is deployed for these multi-core architectures by orchestrating task execution and paging allocations while adapting to system loading

- Power cost of required IT in enterprise decision support systems motives optimizing their energy use without sacrificing performance by database software. Optimized solution is modulated by the workloads. Holistic measurements of an audit-class system running the TPC-H decision support benchmark at 300GB scale are presented

- Cache power reduction technique “Way Guard” that reduces energy of set-associative caches by segmented counting bloom filter

- Way-Tagged Cache architecture for high performance microprocessors lowers the energy consumption of the soft error required write-through policy deployed caches